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DIGITAL 8000 SERIES TTL/MSI

SEVEN SEGMENT DECODER/DRIVER

8T04
8T05
8T06

INTRODUCTION

The Signetics' 8T04/5/6 are monolithic MSI seven segment decoder/drivers that have been designed with TTL techniques. They consist of the necessary logic to decode a 4-bit BCD input to provide the appropriate outputs to drive seven segment digital display devices. Numerals 0-9 as well as selected signs and letters can be decoded for driving the following types of displays:

- Light emitting diodes displays (LEDs)
- Incandescent displays
- Interface transistors and SCRs
- Relays

The three decoders differ basically in the electrical characteristics of the output transistors and their logical activating level. Figure 1 shows a composite logic diagram. The 8T04 has "active low," high current sink open collector outputs for driving indicators directly. The 8T05 has "active high" outputs with internal pull-up resistors to provide sufficient drive current to discrete transistors, SCRs and other interface elements as well as Utilogic NOR and OR gates. The 8T06 also offers "active high" outputs but these are of the open collector type for maximum versatility in a variety of current source applications.

LOGIC DESCRIPTION

A composite truth table (Table I) has been arranged to show the response of the 8T04/5/6 seven-segment decoder /drivers to a 4-bit binary input code. When neither of the auxiliary inputs are activated, a BCD code on the inputs (a, b, c, d) conditions the outputs (A through G) corresponding to a standard seven-segment layout as shown in Figure 2 such that numerals 0-9 can be displayed. Furthermore, any non-BCD input is defined as well such that selected signs and letters may be displayed in accordance with Table I.

Auxiliary terminals are provided for maximum versatility. A ripple blanking input (RBI) and a ripple blanking output (RBO) are used to suppress leading and trailing edge zeros in multidigit displays. In addition, the internal logic design allows the ripple blanking output to serve as a blanking input as well and is therefore designated as RBO/BI. This blanking input (BI) overrides the ripple blanking signal and may be used in various blanking and intensity modulation applications.

The lamp test (LT) input is independent of any other input and may be activated at any time. This input allows the integrity of the display to be checked by overriding all other input states.

LOGIC DIAGRAM

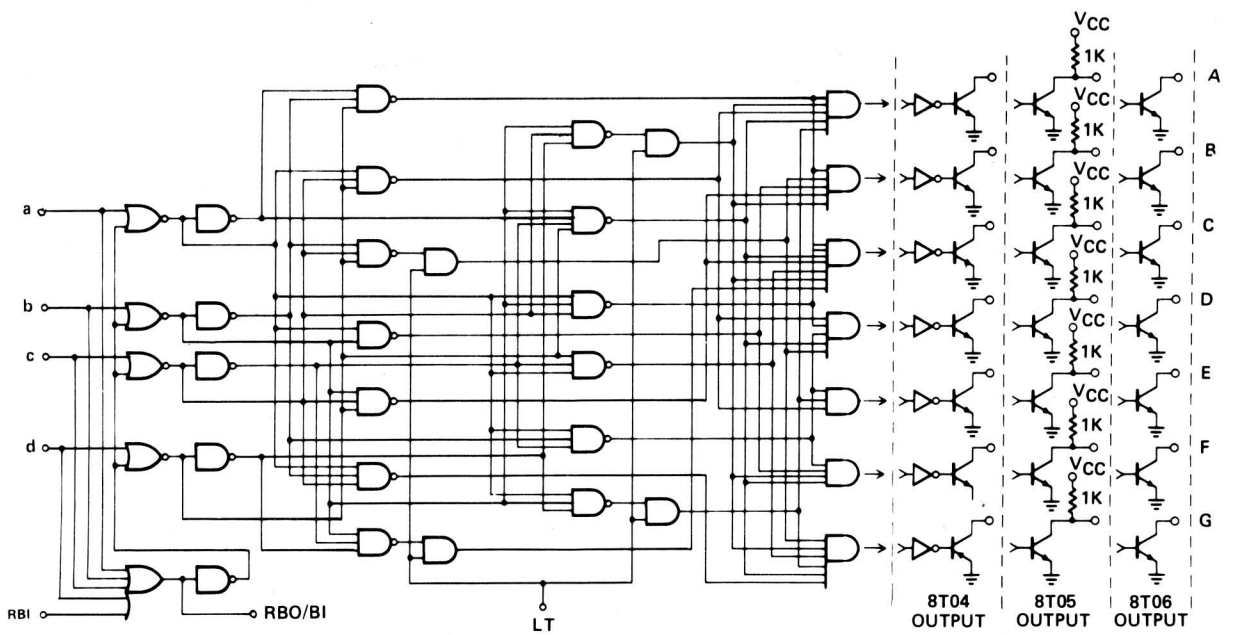
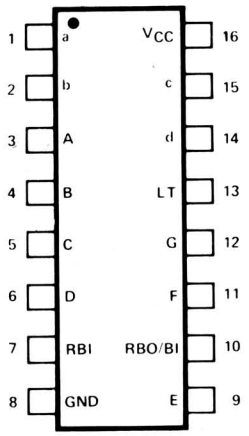


FIGURE 1

PIN CONFIGURATION AND 7–SEGMENT LAYOUT



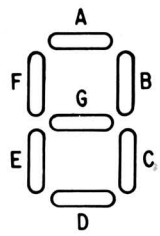


FIGURE 2

Where: a, b, c, d are the BCD inputs to the decoder/driver
A, B, C, D, E, F, G are the seven-segment outputs in accordance with the standard layout as shown.

RBI = Ripple Blanking Input
RBO/BI = Ripple Blanking Output/Blanking Input
LT = Lamp Test

TRUTH TABLE

TABLE 1

INPUTS						BI/RBO	OUTPUTS							OUTPUTS							DISPLAY CHARACTER
INPUT CODE				LAMP TEST	RBI		OUTPUT STATE							OUTPUT STATE							
d	c	b	a	LT		NOTE	A	B	C	D	E	F	G	A	B	C	D	E	F	G	
X	X	X	X	0	X	X	0	0	0	0	0	0	0	1	1	1	1	1	1	1	8
X	X	X	X	1	X	0 Note 1 & 2)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	BLK
0	0	0	0	1	0	0 (Note 2)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	BLK
0	0	0	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0
0	0	0	1	1	X	1	1	0	0	1	1	1	1	0	1	1	0	0	0	0	1
0	0	1	0	1	X	1	0	0	1	0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	X	1	0	0	0	0	1	1	0	1	1	1	1	0	0	1	3
0	1	0	0	1	X	1	1	0	0	1	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	X	1	0	1	0	0	1	0	0	1	0	1	1	0	1	1	5
0	1	1	0	1	X	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	6
0	1	1	1	1	X	1	0	0	0	1	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	X	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	X	1	0	0	0	1	1	0	0	1	1	1	0	0	1	1	9
1	0	1	0	1	X	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	-
1	0	1	1	1	X	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	BLK
1	1	0	0	1	X	1	0	0	0	1	0	0	0	1	1	1	0	1	1	1	°
1	1	0	1	1	X	1	1	1	0	1	1	1	1	0	0	1	0	0	0	0	,
1	1	1	0	1	X	1	1	1	1	0	0	0	1	0	0	0	1	1	1	0	⌐
1	1	1	1	1	X	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	BLK

NOTE:

1. RBO/BI used as input
2. RBO/BI should not be forced high when a,b,c,d, RBI terminals are low, or damage may occur to the unit.
3. * Comma
4. X = Do not care, either "1" or "0"

TERMINAL CHARACTERISTICS

Since these 7-segment decoder/drivers are useful in many applications and interfacing situations involving bipolar as well as MOS circuits, it is important to have a complete understanding of the 8T04/5/6 characteristics.

The data inputs as well as the RBI input are TTL type base-emitter diodes. Clamp diodes are employed to prevent ringing that may occur on long interconnect lines. The equivalent circuit is shown in Figure 3.

The RBO/BI signal is generated as shown in Figure 4. When a BCD zero has been received at the data inputs with the RBI input being low, transistor Q turns on and the collector pulls the BI input low internally. Since the RBO/BI terminal may be grounded at any time, an overriding blanking signal can be supplied externally. To avoid forcing the collector high when Q is activated, the BI input should be driven by an open collector device such as an 8891.

The output transistors of the 8T04 and 8T06 are open collector devices. It can be seen from the equivalent circuit in Figure 5 that because of the collector-substrate isolation diode the output should not be taken more negative than 0.5V without current limiting. The output leakage for the 8T04 and 8T06 is specified at 100μA with 6V applied. Because collector breakdown typically occurs above 15V, an application may be considered with output voltages higher than 6V but below breakdown when using a selected device. In that case, current limiting to about 10mA should be employed to avoid excessive power dissipation in the output transistor.

The equivalent circuit for the 8T05 output which has an internal diffused pullup-resistor is shown in Figure 6. In interfacing it should be noted that the output will clamp at one diode drop above V_{CC}.

To allow judicious tradeoffs in designs, typical characteristics for current source and sink capability are given for the respective devices in Figures 7 through 9.

EQUIVALENT CIRCUITS

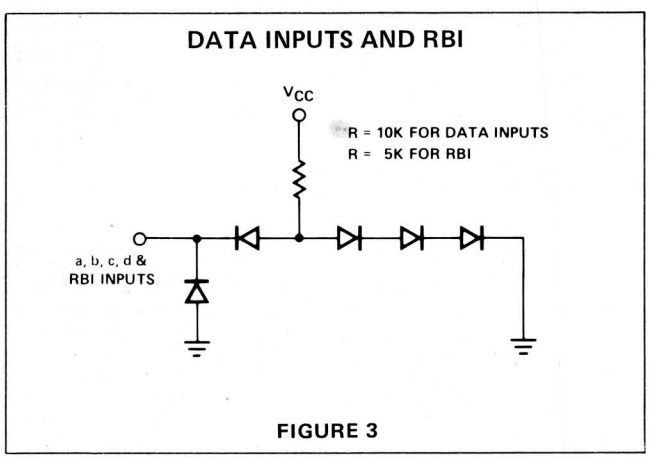


FIGURE 3

EQUIVALENT CIRCUITS (Cont'd.)

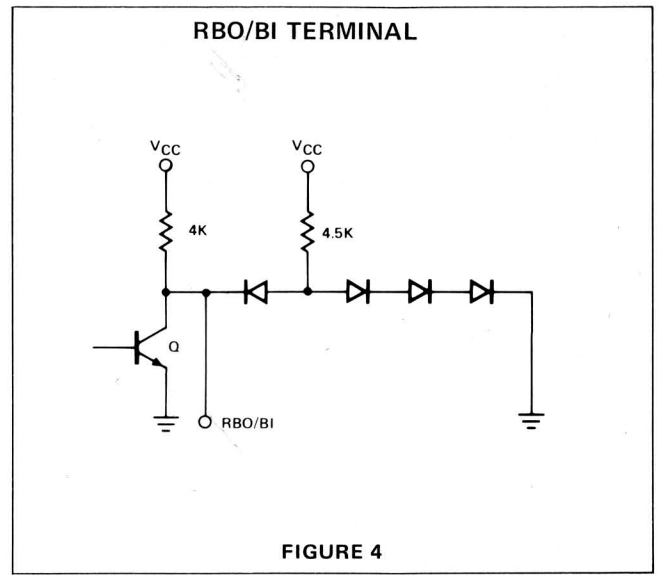


FIGURE 4

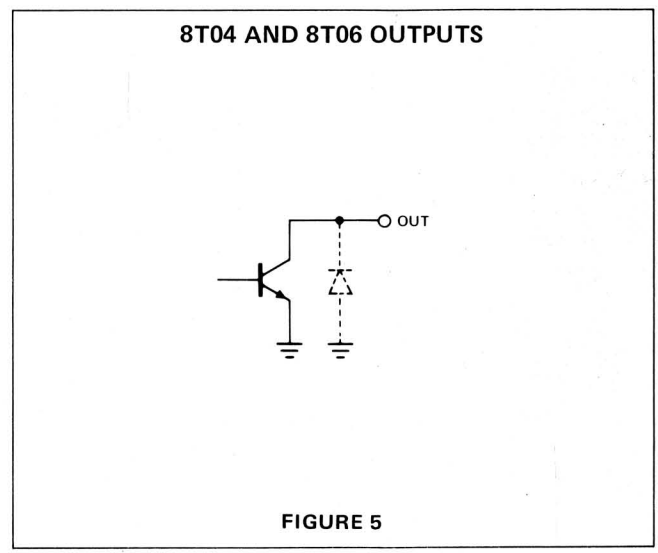


FIGURE 5

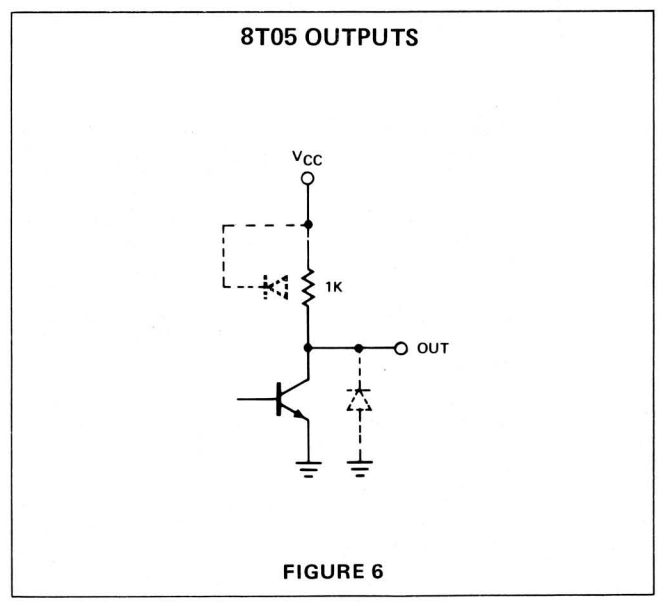


FIGURE 6

TYPICAL CHARACTERISTICS

TYPICAL CURRENT SINK CHARACTERISTICS OF THE 8T04 & 8T06 (OUTPUTS A THROUGH G)

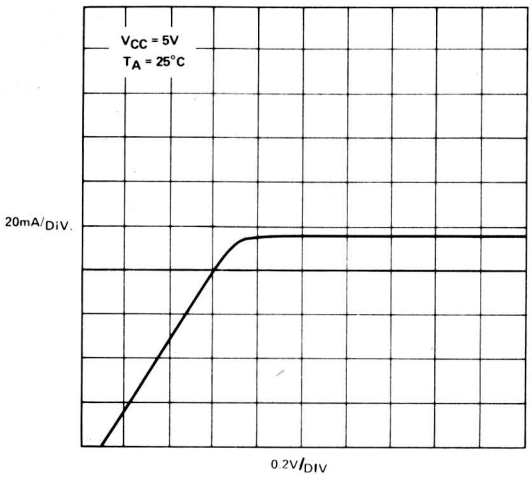


FIGURE 7

TYPICAL CURRENT SINK CHARACTERISTICS OF THE 8T05 (OUTPUTS A THROUGH G)

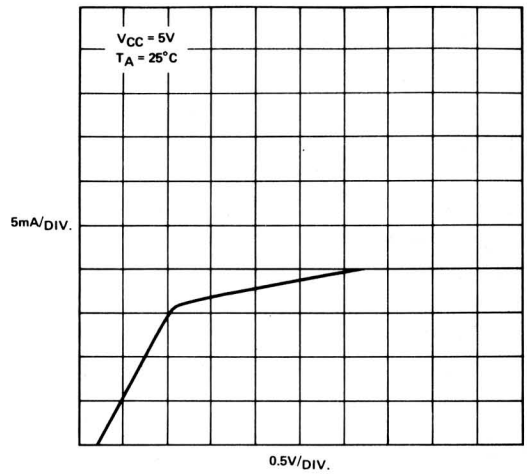


FIGURE 8

TYPICAL CURRENT SOURCE CHARACTERISTICS OF OF THE 8T05 (OUTPUTS A THROUGH G)

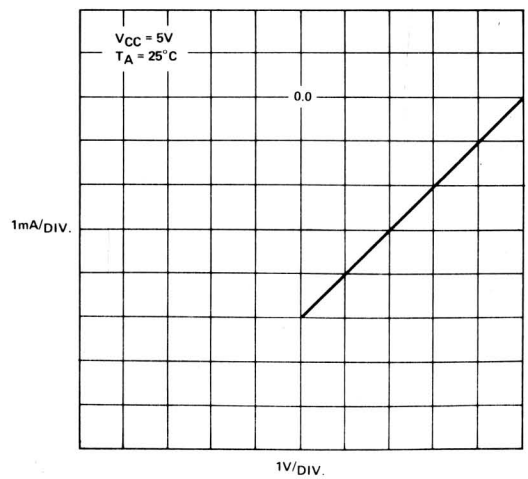


FIGURE 9

OUTPUT SPECIFICATIONS

Table 2 is designed to assist in selecting the proper decoder for a desired application. The 8T04 has "active low" outputs. Thus it is suited for high current sink applications where the driver has to sink current from a load. However, the 8T05/6 devices have "active high" outputs, meaning that they are well suited for applications where current has to be sourced to the load. This may be done either through the internal pullup resistor (8T05) or through an externally provided element (8T06) when high current is required.

OUTPUT SPECIFICATIONS OF THE SEVEN SEGMENT DECODER/DRIVER

TABLE 2

PART NO.	OUTPUT STRUCTURE	ACTIVATING LEVEL	CURRENT SINK SPECIFICATIONS	OUTPUT "1" LEAKAGE OR CURRENT SOURCE SPEC.
8T04	OPEN COLLECTOR	LOW	40mA @ .4V	100μA @ 6V
8T05	PASSIVE PULL–UP	HI	.5mA @ .3V	–2.3mA @ 1V; –500μA @ 4.1V
8T06	OPEN COLLECTOR	HI	40mA @ .4V	100μA @ 6V

APPLICATIONS

Several techniques are used for driving digital display devices. The most straightforward application is to use one 7-segment decoder/driver for each display. Because a blanking provision is available, the displays may be strobed for low power operation or variable light intensity.

Depending on the existing circuitry it may also be advantageous to time-share one decoder among several or all displays. In such a multiplexed operation, suitable timing and decoding are incorporated such that only one display will be illuminated at a time. This strobed operation is done at a repetition rate high enough to appear flicker free to the eye.

LIGHT EMITTING DIODE DISPLAY

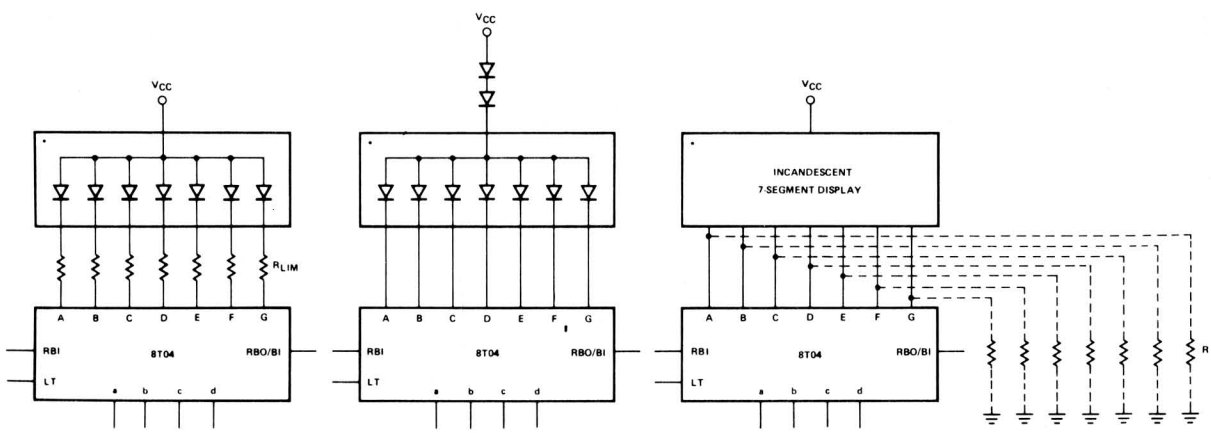
Several light emitting diode displays (LEDs) have common anodes. These require a decoder/driver with "active low" outputs and high current sink capability. Similar requirements exist for incandescent displays and the 8T04 is ideal for these applications without the need for interface transistors.

The turn-on characteristics of the display are important when interfacing with the decoder/driver. Figure 10a shows the 8T04 driving a light emitting diode display. Since the forward drop of the LEDs may be slightly unequal, they may exhibit current-hogging if driven from a common voltage source. Thus, to obtain equal brightness in the display segments, LED manufacturers generally advise to use individual current limiting resistors. However, LED displays have been used successfully without an apparent difference in brightness as shown in Figure 10b. Current limiting resistors are therefore eliminated.

An important consideration for incandescent displays is inrush current through a cold filament, since it could be 10 times as high as the rated operation current. Figure 10c shows the 8T04 driving an incandescent seven-segment display and if the external resistors R (dotted connections) are used, a small current is allowed to flow through the lamps during the off-state, keeping the filaments warm. Thus, inrush current effects are minimized, prolonging the life of the lamp.

Surge current protection of the driver is not required in this context because the current-sink capability of the output transistors is beta-limited. Typical tests have shown that the output characteristics flaten out at about 80mA (Figure 7), therefore setting a natural limit to inrush current. Consequently, no damage to the driver will be sustained when driving lamps that have steady state currents falling within the defined output drive capability of the seven-segment decoder/driver.

8T04 DRIVING 7–SEGMENT DISPLAY



a) LED DISPLAYS WITH INDIVIDUAL LIMITING RESISTORS

b) LED DISPLAY WITH SERIES DIODES

c) INCANDESCENT DISPLAY

NOTES:

1. LED displays such as: Litronix Data Lit 10 ,Monsanto Man 1, Opcoa SLA 1.
2. Incandescent displays such as: Pinlites "Lite Pak" ,RCA Numitron DR 2000, Readouts Inc. Series 5.

FIGURE 10

8T05 INTERFACING APPLICATION

The 8T05 has "active high" outputs with internal 1K ohm pullup such that external buffers may be driven directly without the need for additional components. Hence, it is easy to interface with driver transistors that may be required for very high current incandescent lamps or high voltage interfaces to fluorescent or gas discharge displays.

Should the need exist to interface with logic circuits, one standard TTL load (-1.6mA @ .4V) can be driven. Utilogic OR and NOR gates have base inputs and only require 180μA input current, thus allowing a fanout of 10. The 8T05 can also be used to drive SCR's such as to interface the 7-segment decoder with electroluminescent displays that require high AC voltages. Such an application is shown in Figure 11.

If additional drive current is required from the 8T05 it is possible to add external resistors from V_{CC} to the 7-segment outputs of the decoder/driver. Since the minimum value of the total pullup resistors is constrained by the current sink capability of the output transistors, it is advantageous to use the 8T06 which is pin compatible and designed for high current source applications.

LED DISPLAY USING THE 8T06 DRIVER

Monolithic light emitting diode displays are presently manufactured with common cathodes which require a driver with current source capability. The 8T06 7-segment decoder/driver has been designed specifically to drive common-cathode LEDs, and employs open-collector transistors for maximum versatility. External pullup resistors must be used to limit the source currents in accordance with the LED manufacturers specifications and the intended usage of the display. A typical application of the 8T06 driving a common cathode LED is shown in Figure 12. Because of the 8T06's high current sink capability (40mA), it can be used as a LED driver for pulsed operation or in the multiplex mode where only one decoder/driver is used for a multidigit display. Figure 16 shows such an arrangement in detail.

8T05 DRIVING ELECTRO–LUMINESCENT DISPLAY

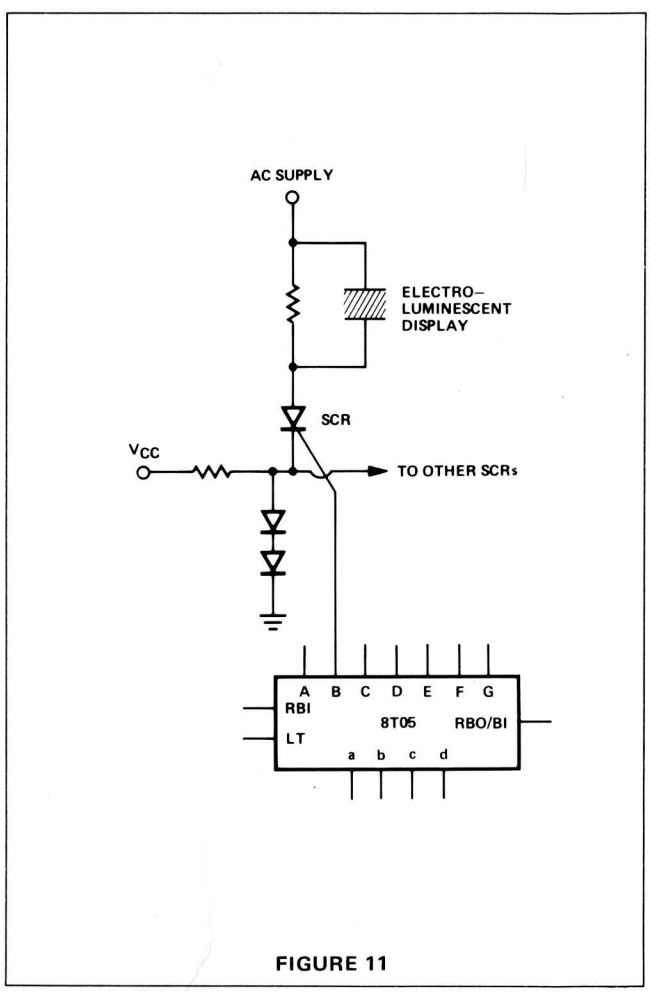


FIGURE 11

8T06 DRIVING MONOLITHIC LED DISPLAY

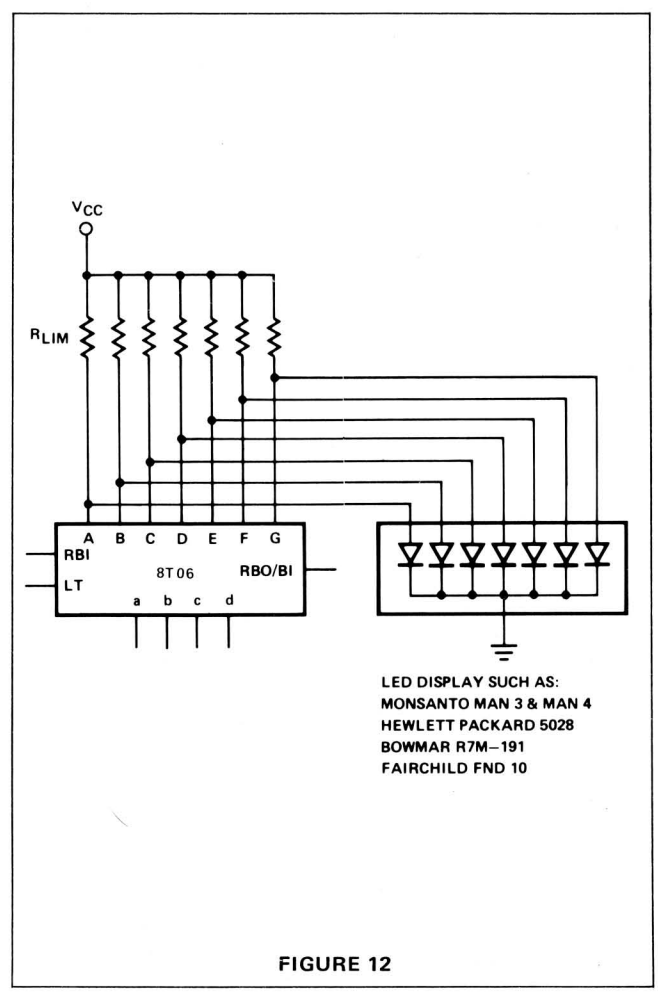


FIGURE 12

RIPPLE BLANKING AND INTENSITY MODULATION APPLICATION

The provision for automatic blanking of leading and/or trailing edge zeros is a very useful feature in multi-digit displays. By blanking insignificant zeros, any display can be easily read. For example, in a ten digit display a mixed integer fraction (000457.1800) would be displayed as 457.18.

To suppress leading edge zeros, the Ripple Blanking Output (RBO) of a decoder is connected to the Ripple Blanking Input (RBI) of the next lower stage device. In the total display, the most significant bit's RBI input is connected to ground to enable the blanking command to ripple through if that decoder is addressed with a BCD zero (0000). It is common practice to tie the least significant bit's RBI input to V_{CC} since it is generally not desirable to blank the least significant integer. Figure 13 shows an example for n-integers.

Trailing edge zero suppression is needed when the fractional part of a number has to be conditioned similar to the example above. Because it is desirable to retain the first zero after a decimal point, the RBI input of the most significant digit in the fractional part should be tied to V_{CC}.

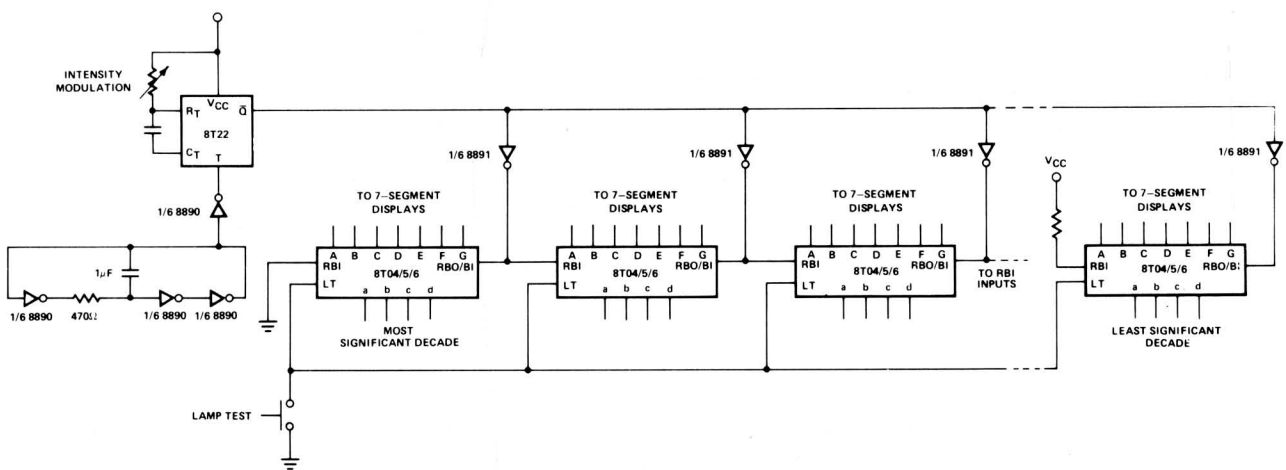
The RBO terminal may also be used as an overriding blanking input (BI) in a variety of inhibiting and strobing operations that may be associated with the outputs. An extremely useful application also shown in Figure 13 is intensity modulation. The variable duty cycle multivibrator can be used for low duty cycle strobed operation or display dimming.

FLOATING DECIMAL POINT APPLICATION

The ripple blanking shown in the previous example may be extended to an application such as desk calculator displays where the position of the decimal point can be selected. In Figure 14 a few additional gates are used such that the decimal point can be fixed by means of a "select line". To select the decimal point position, the corresponding select line must be at a logical "1" while all the other select lines are held at a logical "0".

As a result, the least significant integer as well as the most significant part of the fraction will not be blanked (since 0.0 may occur which is a meaningful result) but any other leading or trailing edge zero will be blanked to obtain an easily readable display.

SEVEN–SEGMENT DISPLAYS FOR n–INTERGERS

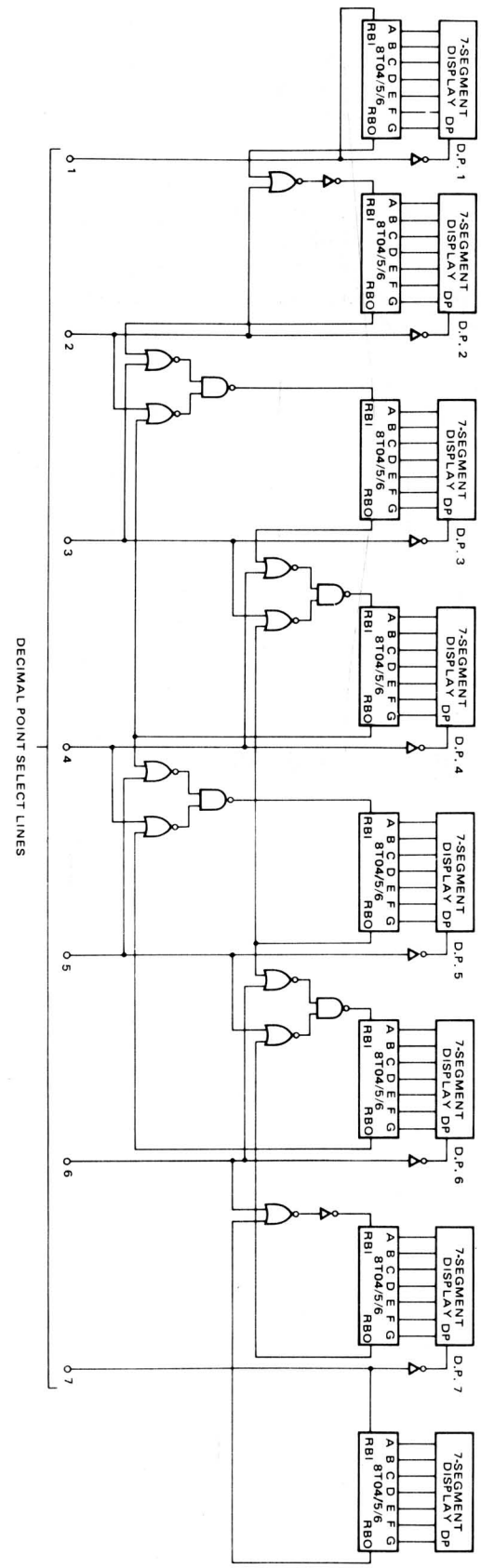


NOTES:

1. RIPPLE BLANKING– Automatically suppresses all unnecessary zero's which may be either those preceding the first significant digit (as shown) or those trailing the last significant digit after a decimal.
2. LAMP TEST– Overrides all output states generated from input codes.
3. INTENSITY MODULATION– Turns on the seven-segment displays only for the pulse duration. This may be used as a lamp intensity control or for low duty cycle pulsed operation.

FIGURE 13

8 DIGIT DISPLAY WITH FLOATING DECIMAL POINT AND RIPPLE BLANKING



NOTES:

1. To select a decimal point, the corresponding select line must be at a logical "1" while all the remaining select lines are held at logical "0"s.
2. Gates used: 8880 Quad 2-Input NAND Gate; 8885 Quad 2-Input NOR Gate; 8890 Hex Inverter.

FIGURE 14

MULTIPLEXING OF DISPLAYS

When designing with multidigit displays, two distinctly different approaches may be taken when interfacing the displays with the decoder/driver circuitry. The standard solution would be to use one decoder/driver for each digit in the display. As the number of digits increases it is generally advantageous to time-share one decoder/driver among all digits or groups of digits as shown in Figure 15.

The choice of one technique over the other depends heavily on the application. In particular, the total hardware cost, package count, and power consumption in a multiplexed display system are not only influenced by the number of digits that time share a decoder/driver, but also if the BCD data is available in serial or parallel form.

The principal argument that may be advanced for multiplexing of displays is generally one of economics although a considerable power savings may result as an added benefit. For example, LED 7-segment displays have a high persistence allowing them to be strobed with a very low duty cycle which is an important consideration for battery powered equipment.

A circuit for multiplexing a counter display is shown in Fig.16. By using the 8T10 Quad-D-Type Bus Flip-Flop with tri-state outputs, for storage buffers, the digit information of all counter outputs can be bussed onto common BCD lines. Thus, the design of a multiplexed display is greatly simplified. In this example, common anode displays are driven by an 8T04. Current limiting resistors are used in each 7-segment line to assure equal brightness even if the LED turn-on voltages are slightly unequal.

The 8250 Octal decoder that selects the BCD information from 8T10 buffers and corresponding digit drivers is indexed by an 8293 counter in the divide-by-8 mode. A 1kHz repetition rate for the multiplex oscillator was chosen which is high enough to make the display appear flicker free to the eye.

Notice that the 8T04 and 8T06 are very well suited for strobed operation of displays. Because of their high current sink capability, displays can be pulsed with high currents and low duty cycles, enhancing the apparent brightness of the displays and saving power at the same time. Use of the 8292 and 8293 counters further reduces system power consumption.

GENERALIZED MULTIPLEXING SCHEME FOR DISPLAYS

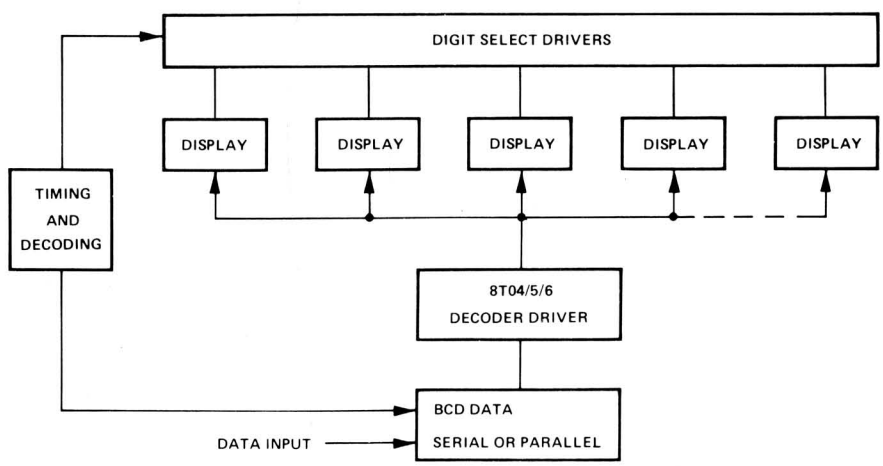
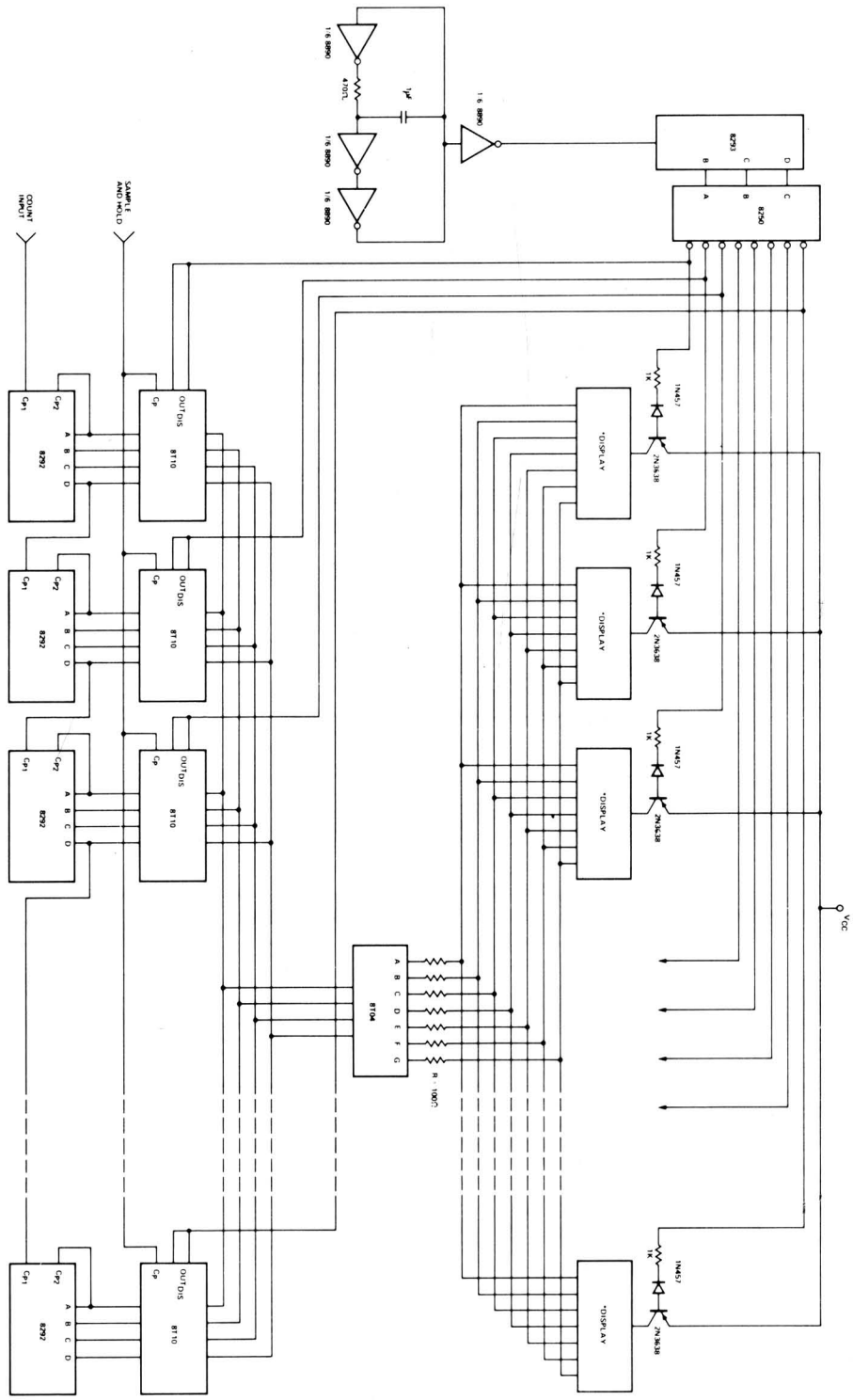


FIGURE 15

MULTIPLEXING EIGHT LED DISPLAYS



*Led displays such as Litronix Data Lit 10, Monsanto Man 1, Opcoa SLA 1

FIGURE 16

8T09 QUAD BUS DRIVER/ 8T10 QUAD D-TYPE BUS FLIP-FLOP

INTRODUCTION

Designers of digital systems have been using open-collector TTL logic for many years because its wire-OR capability is a powerful design tool. With the addition of an external pull-up resistor, many open-collector outputs can be connected onto a common bus, resulting in a considerable savings of hardware and speed advantages over conventional approaches. Particularly in computer design where bus-organized systems architecture prevails, Signetics open-collector MSI and open-collector gates are used extensively.* There are applications, however, especially in systems with electrically short interconnects, such as on-card bussing and areas of modular systems design, in which performance can be improved by two new TTL compatible bus driver circuits that have been developed by Signetics.

SIMPLIFIED TRI–STATE BUS DRIVER

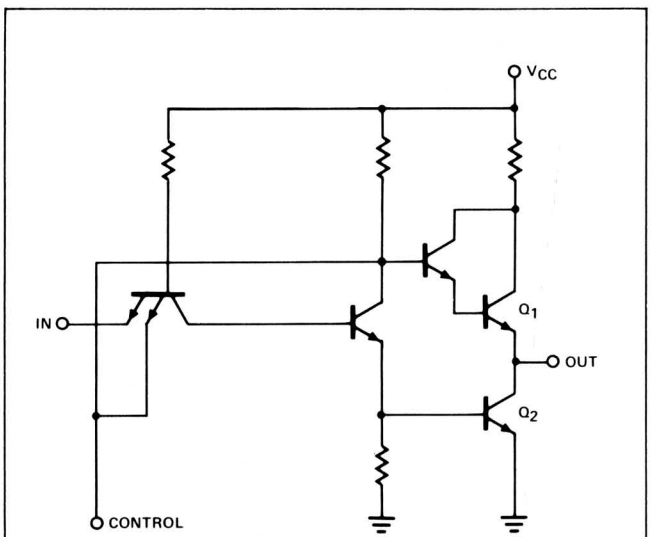


FIGURE 1

These designs, the 8T09 Quad Bus Driver and the 8T10 Quad D-Type Flip-Flop combine the advantages of active pull-up TTL with the wire-OR capability of open-collector ICs. As shown in the simplified circuit diagram in Figure 1, a bus driver can be designed to exhibit three distinct output states. Such a tri-state device is unique in that it may act as a normal TTL gate with low impedance logical "1" and logical "0" levels as long as the control line is high. If the control line is grounded, drive current is removed from the active pull-up Darlington-structure and a third, high impedance output state results. Since in that third state both output transistors (Q_1 and Q_2) are biased in the off-condition, only microampere leakage current will have to be supplied to the device by an active bus driver tied to the same bus.

*Unified Bus Maximizes Minicomputer Flexibility, ELECTRONICS, December 21, 1970.

Two integrated circuits, the 8T09 Quad Bus Driver and the 8T10 Quad D-Type Bus Flip-Flop that have tri-state outputs will be described here and applications such as bus organized information transfer, modular systems design and multiplexing will be discussed.

8T09 QUAD BUS DRIVER

The 8T09 Quad Bus Driver is a hardware realization of the tri-state bus driver concept. It may be seen from the circuit diagram in Figure 2 that depending on the state of the disable input, a driver will either act as a high speed inverting buffer or will exhibit a high impedance "OFF" state similar to an open-collector gate.

CIRCUIT SCHEMATIC OF 1/4 8T09

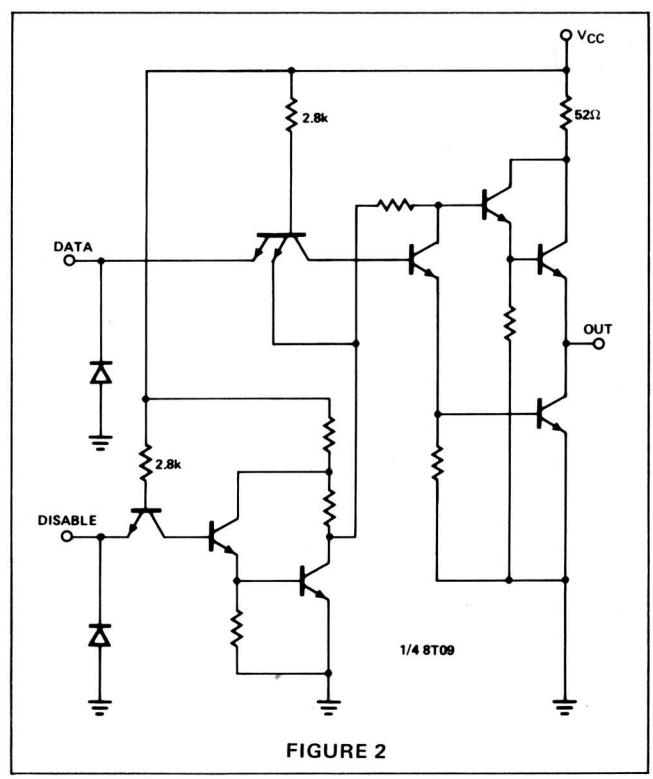


FIGURE 2

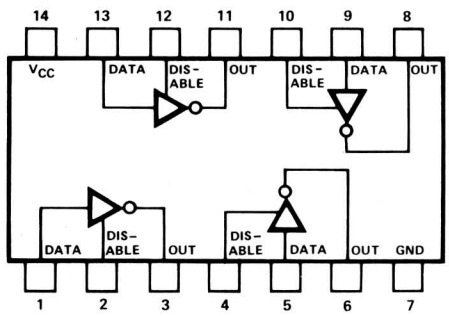
The Darlington pull-up structure at the output provides high current source capability (guaranteed 5.2mA at 2.4V) when driving a data bus, thus allowing high speed operation even when driving heavy capacitive loads. The current sink capability of the bottom transistor is 2-1/2 times that of a standard TTL gate (guaranteed 40mA at 0.4V) making the device very versatile in a variety of interface situations.

Figure 3 shows the logic diagram and truth table of the 8T09. A logical "0" on the disable input makes the bus-driver a high speed inverting buffer with low impedance logical "1" and logical "0" states. To place the output in the high-Z disable state, the disable signal has to be a logical "1". This fact is beneficial when considering fail-safe operation since removal of the disable signal, which may happen accidentally, will not damage any driver. The inputs of the 8T09s are diode clamped to discriminate against negative ringing.

APPLICATIONS OF THE 8T09 QUAD BUS DRIVER

Tri-state outputs combined with high-speed and high output current capability in both the logical "1" and logical "0" level allow the 8T09 to be used in a variety of bus-organized systems and wired-OR applications.

LOGIC DIAGRAM AND TRUTH TABLE OF THE 8T09



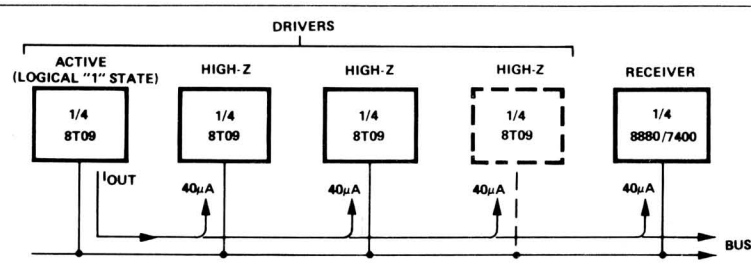
DATA	DISABLE	OUTPUT
0	0	1
1	0	0
0	1	HI-Z
1	1	HI-Z

FIGURE 3

In existing logic designs, the 8T09 may be used to replace open-collector devices to increase systems speed by as much as a factor of ten. This speed improvement is accomplished by the short propagation delays associated with the data path (10ns max.) and the excellent capacitive drive capability of the 8T09. As an added benefit, pull-up resistors are no longer necessary, which will also have an impact on new systems designs where bussing can be used.

Figure 4 illustrates the excellent drive capability of the 8T09. Since a disabled bus-driver is in the high-Z state and only requires 40uA leakage current, as many as 129 disabled drivers and a standard TTL gate (8880 or 7400)can be driven by one 8T09 in the logical "1" state. The 8T09 also has high current sink capability in the logical "0" state, making many other driver and receiver combinations possible. Of special interest is a bidirectional data bus as indicated in Figure 5. When using standard TTL gates as receivers such as 8880s and 7400s, as many as 25 receiver/transmitter pairs may be tied onto the same bus without exceeding the logical "0" drive capability of the 8T09.

LOGICAL "1" DRIVE CAPABILITY OF THE 8T09



I_{HI-Z}(LEAKAGE) 40μA X 129 DRIVERS = 5.16mA
$I_{IN(1)}$ LOGICAL "1" INPUT CURRENT 40μA = .04mA
5.20mA

FIGURE 4

BIDIRECTIONAL DATA BUS

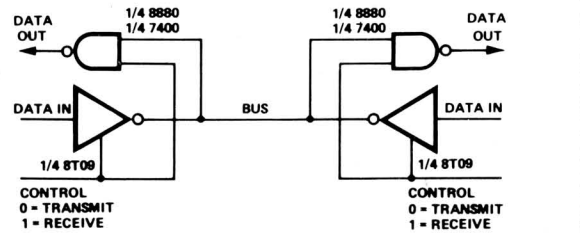


FIGURE 5

Standard MSI circuits may be adapted easily to bus-organized systems. By using the 8T09 as shown in Figure 6, a minicomputer can be designed using a single high speed bus. An arithmetic logic unit (74181), scratch pad memory (8225) and I/O devices (through 8233 multiplexers) may communicate directly. Moreover, microprogrammed instructions from a 1024 bit tri-state FROM (8229) may be put on the bus with out need for an interface.

8T09 IN A BUS–ORGANIZED MINICOMPUTER

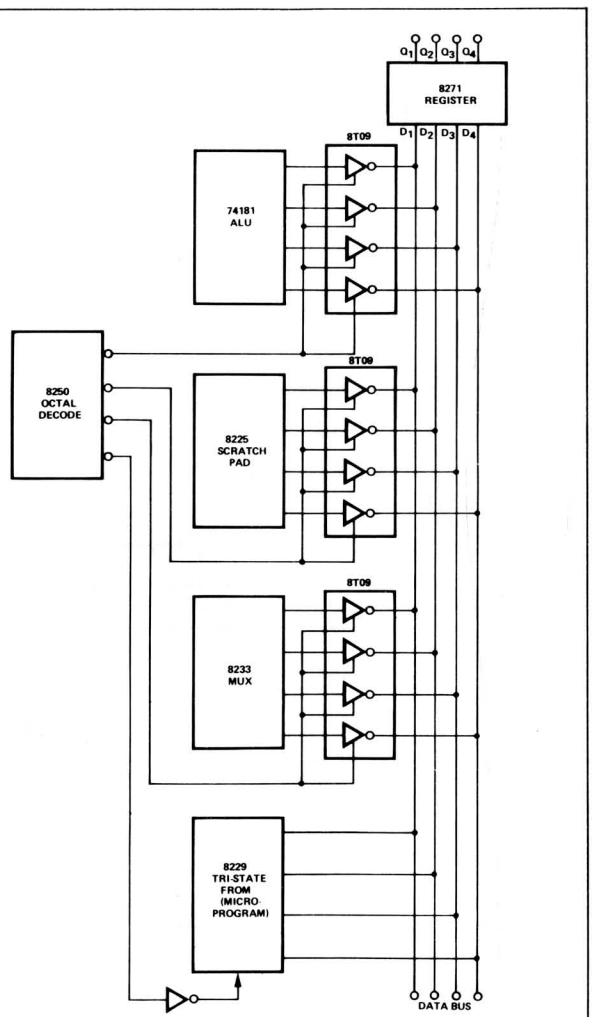


FIGURE 6

8T10 QUAD D–TYPE BUS FLIP–FLOP

A logical extension of the 8T09 bus driver is the 8T10 Bus Flip-Flop. In one integrated circuit a Quad D-Type flip-flop has been combined with tri-state output drivers for use in bus organized systems. As shown in Figure 7, the outputs are disabled, i.e., switched to the high impedance state when one or both of the inputs to the output disable NOR-gate are a logical "1". Having two output disables facilitates X - Y decoding with active low decoders such as the 8250/51/52. Since the outputs will only be enabled with a logical "0", fail-safe operation in bus-organized systems is assured should the disable signal be removed such as is the case when the disable driver card is removed for some reason.

LOGIC DIAGRAM OF THE 8T10

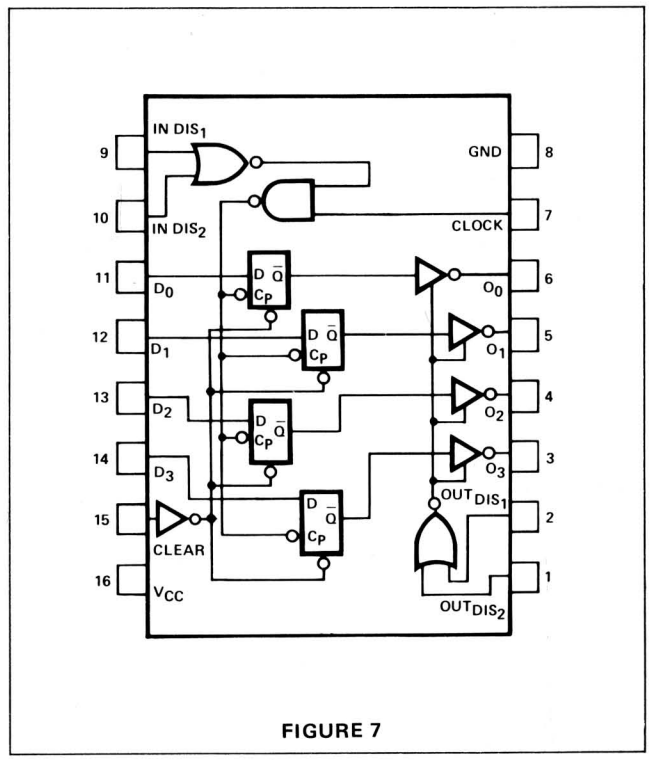


FIGURE 7

All four D-Type flip-flops operate from a common clock, and the data is transferred from the input to the output on the low-to-high transition of the clock pulse. The minimum clock-pulse width is 12ns. Since the clock pulse and the input disable are gated through a common NAND-gate, the input should not be enabled while the clock is high to avoid false triggering. Input enable should be defined before the clock rises, but may change any time thereafter.

With one or both of the input disable inputs at a logical "1" the flip-flops are in the hold mode and will store the information clocked in prior to the disable signal. A common clear input has also been provided. All flip-flops will be reset upon application of a logical "1" clear pulse at least 15ns wide.

TRUTH TABLE OF THE 8T10

D_n	IN_{DIS}	OUT_{DIS}	OUT_{n+1}
0	0	0	0
1	0	0	1
X	1	0	OUT_n
X	X	1	HIGH Z

FIGURE 8

The "1" level output current from the 8T10 tri-state outputs is the same as the 8T09, thus by the same argument , an 8T10 output can drive 129 8T10s or 8T09s in the high-Z state as well as a standard 8800 or 7400 gate (Ref. Figure 4). The 8T10 outputs have 32mA current sink capability at 0.4V, meaning that up to 20 standard loads can be driven. Therefore, like the 8T09, the 8T10 can be used in a variety of applications where high current sink capability is required. To guarantee trouble-free systems performance, all data and control inputs of the 8T10 are diode clamped to discriminate against negative noise and ringing.

APPLICATIONS OF THE 8T10 QUAD D–TYPE BUS FLIP–FLOP

The buffered tri-state outputs of the 8T10 allow the device to be used directly with other 8T10s in high speed bus-organized systems without the need for interface gates or pull-up resistors. Whenever tri-state bus interfaces without storage are desired, the 8T09 may of course be used. The 8T09 bus driver has the same output characteristics as the 8T10 and with slightly higher current sink capability.

MULTIPLEXING OF DATA IN BUS–ORGANIZED SYSTEMS

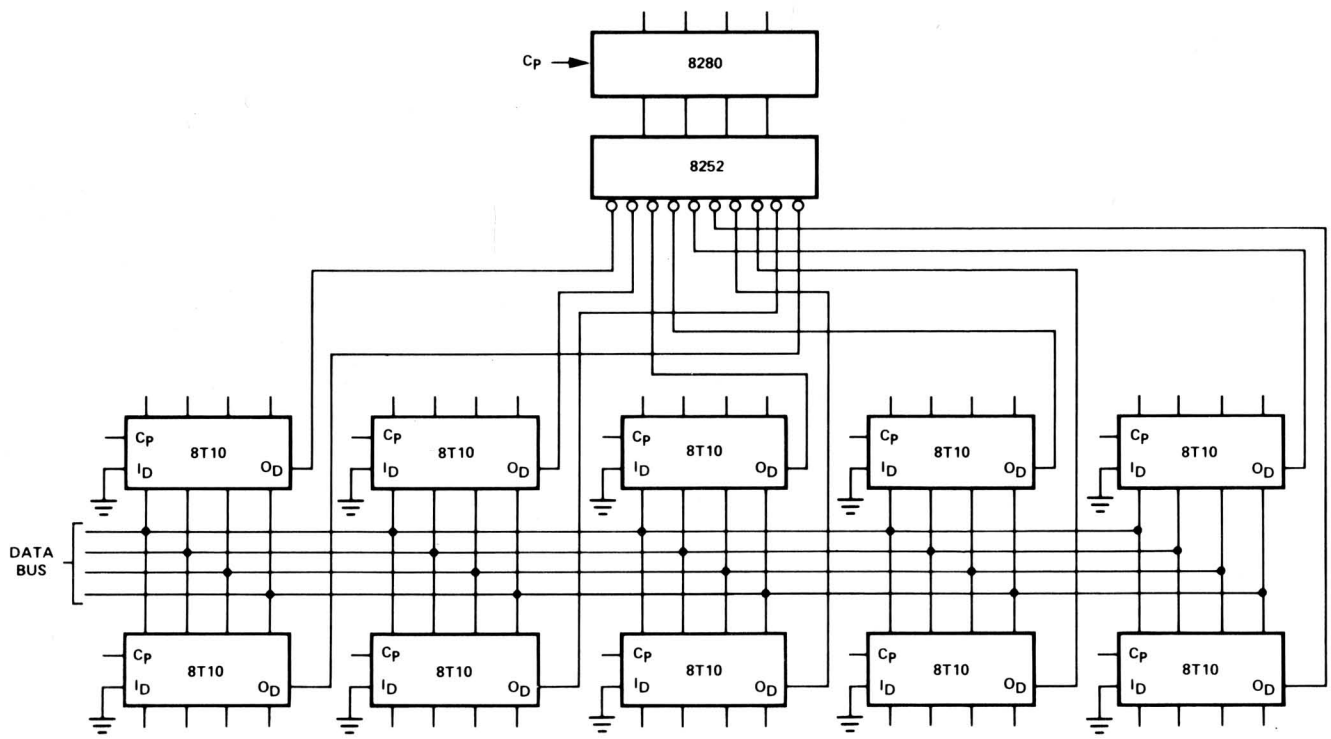


FIGURE 9

Multiplexing of data in bus-organized systems is rather simple, as illustrated in Figure 9. Each 8T10 provides data storage and is selected onto the bus by a logical "0" on both output disable lines. By means of an 8252 one-out-of-ten decoder and an 8280 counter, any one of the 10 bus flip-flop devices can be selected. Should another section of the bus be busy, the 8252 may be blanked, which disables all ten 8T10 devices shown.

As mentioned previously, as many as 129 other 8T10's, as well as a standard TTL receiving gate may be driven by an enabled 8T10. To facilitate output decoding, each 8T10 has a 2-input NOR-gate for the output disable function. As long as either NOR-gate input is high, the 8T10's outputs will be disabled and in the high-Z state. Figure 10 shows how two 8250 one-out-of-ten decoders are used in an X - Y matrix that can select one-out-of-64 8T10s onto the data bus.

X–Y MATRIX FOR SELECTION OF 8T10 BUS FLIP–FLOPS

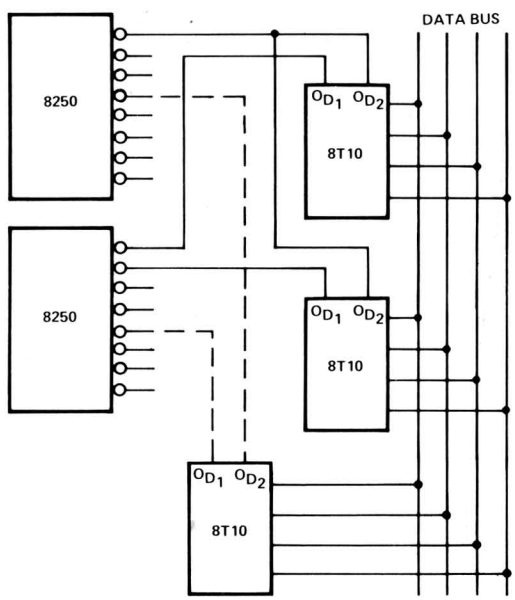


FIGURE 10

Multiplexing of displays is greatly simplified and hardware is significantly reduced when using the 8T10 Quad D-Type Bus Flip-Flop. Figure 11 shows that one decoder driver such as the 8T01 NIXIE decoder/driver or the 8T04/5/6 seven-segment decoder/driver may be time-shared among several displays. If the display is large enough, the digit select drivers and decoding circuitry will cost much less than individual decoder drivers. In addition, strobing displays will result in a net power savings.

MULTIPLEXING OF DISPLAYS USING THE 8T10

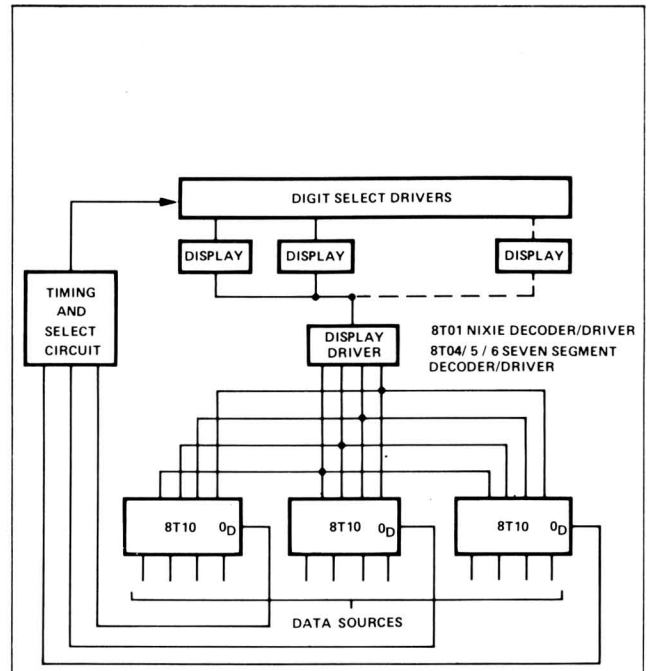


FIGURE 11

The 8T10 may also be configured into a bus-organized register file that can be used in a variety of applications requiring a scratch pad memory. Figure 12 shows such an application. Simultaneous read and write are possible and the memory is easily expanded in word length. Input and output decoding of the 8T10 is simplified because of its NOR-gate input and output disable lines.

SYSTEMS CONSIDERATIONS

The 8T09 and 8T10 bus devices are easy to use but caution should be exercised in systems design with tri-state devices. Because of their high output current capability the 8T09 and the 8T10 should be adequately decoupled just as other TTL drivers, placing a 0.01 to 0.1uf high frequency capacitor as close as possible to the package.

In a system only one tri-state bus device per common bus is allowed to be enabled at a time. It should be realized, however, that in a practical system, control signals may be skewed, creating a slight overlap of the disable signals. Thus it is possible for a transient condition to occur in which two output stages are turned on simultaneously with opposite logic levels. In general, these conditions should be avoided although narrow overlaps of control signals with low duty cycles may not damage any bus drivers and adequate decoupling will handle the surge current demand.

4X4 BUS–ORGANIZED REGISTER FILE

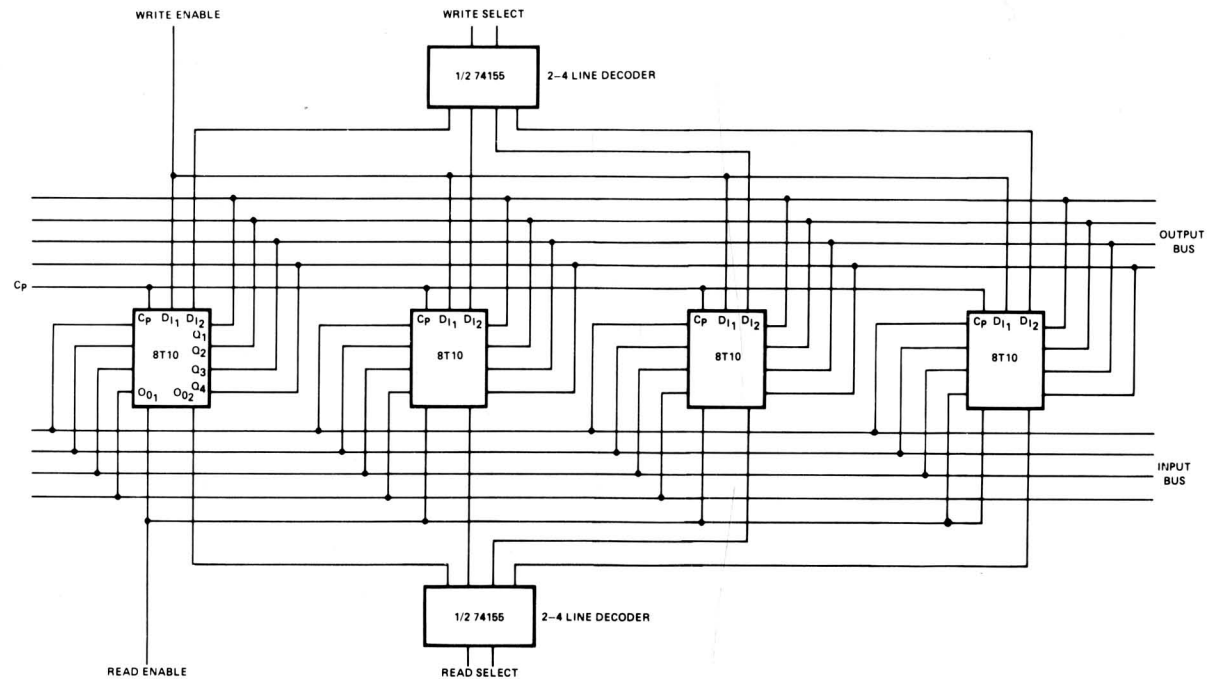


FIGURE 12

8T13 LINE DRIVER/8T14 LINE RECIEVER

8T13 DUAL LINE DRIVER

The Signetics 8T13 is primarily intended for driving low impedance transmission lines such as coaxial cable, twisted pair or ribbon conductors. Both input and output are TTL compatible and the device is operated from a single 5 volt power supply.

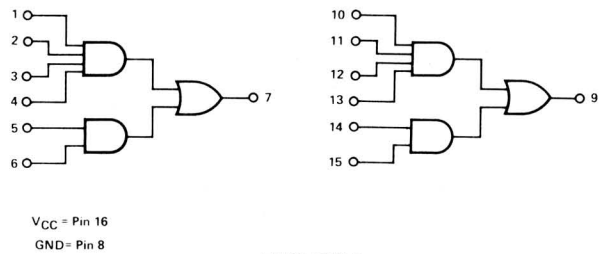


FIGURE 1

LOGIC

The 8T13 contains two AND-OR circuits with one 4-input and one 2-input AND gate for each driver as shown in Figure 1. Unused inputs should be connected to driven inputs where possible to increase circuit speed and to minimize noise coupling into the device.

CIRCUIT DESCRIPTION

The electrical schematic for one of the drivers is shown in Figure 2. The output of the driver is a low impedance emitter follower with built-in short circuit protection. Referring to the circuit, it can be seen that transistor Q_8 will turn on once the output has dropped below approximately two diode drops. Base drive will then be diverted from Q_9 and the output transistor will turn off. Typical output voltage versus current characteristics are shown in Figure 3 over the full temperature range (-55°C to +125°C).

1/2 8T13 LINE DRIVER

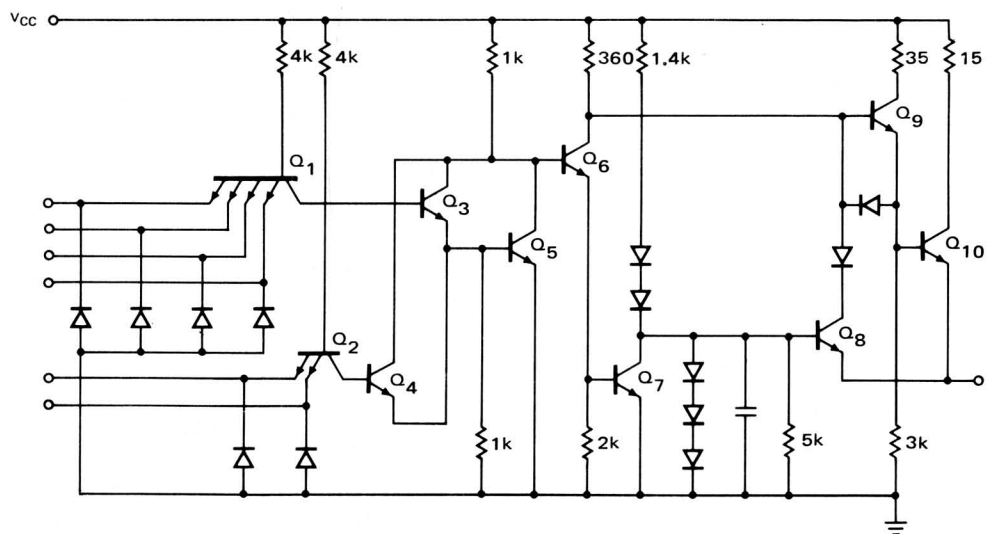


FIGURE 2

The output impedance of the emitter follower output stage during the logic "0" to logic "1" transition is approximately 15 ohms. This low impedance combined with the inherent drive capability of the 8T13 results in an excellent device for driving heavy capacitive loads. Figure 4 shows the typical rise time versus load capacitance for the 8T13 with a 50 ohm pull-down resistor. The output fall time will be governed by the equation: T_f=2.2 RC.

Parallel operation of the 8T13 for additional drive capability can be accomplished. The function obtained is then the logic OR of each output tied to the common bus.

TYPICAL OUTPUT CURRENT VS. OUTPUT VOLTAGE

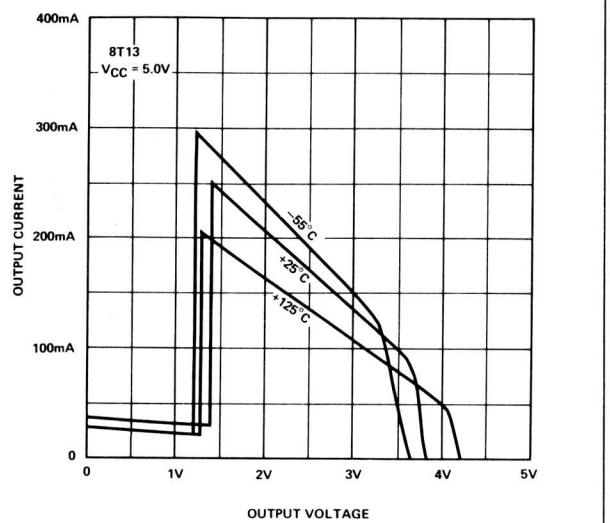


FIGURE 3

TYPICAL RISE TIME VS. LOAD CAPACITANCE

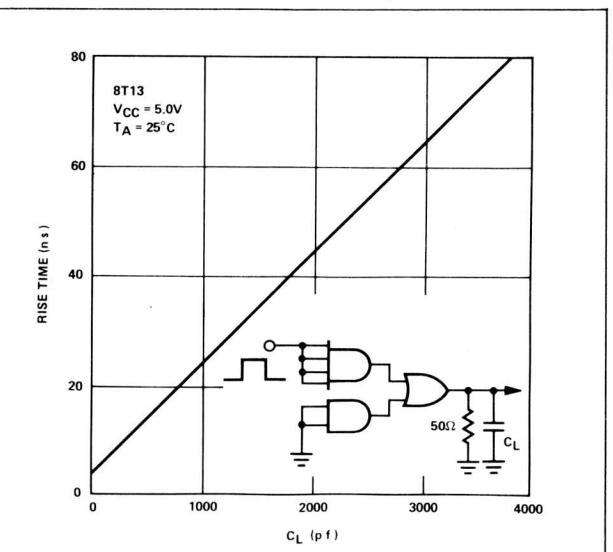


FIGURE 4

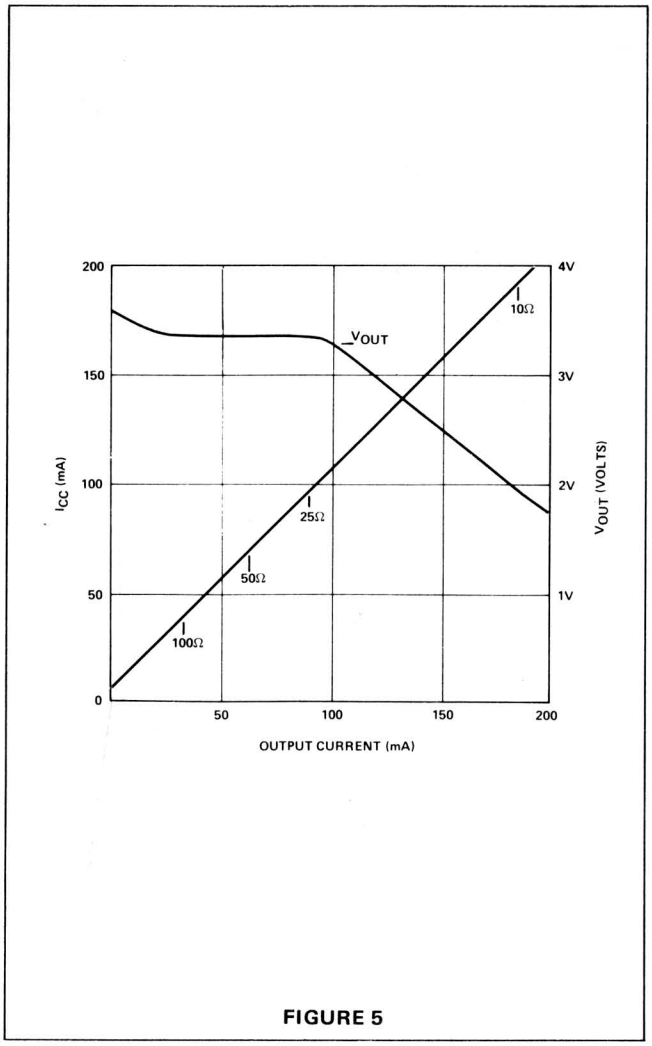


FIGURE 5

POWER DISSIPATION

Typical power supply current and output voltage as a function of load current is shown in Figure 5. For convenience corresponding values of load resistance are also shown. This graph is useful in calculating the total power dissipated by both line drivers in a single package.

Depending upon the output state, the power dissipation of each driver is:

(Logic '1') $P_{diss} = [(V_{CC} - V_{out}) \times I_{out}] + 50mW$

(Logic '0') $P_{diss} = 140mW$

For example, if both drivers in a package are connected to 50 ohm lines but one is turned off (logic '0' state), the total power dissipation would be:

P_{diss} = P_{diss} ('1' state) + P_{diss} ('0' state)

= [(5V – 3.3V) X 65mA] + 190mW

= 300mW

8T14 LINE RECEIVER

The 8T14 was designed to be used at the receiving end of a transmission line for reshaping digital pulses. The device has a built-in hysteresis of 0.5 volt (typical) to discriminate against line reflections and noise. The line receiver is also TTL compatible and operates from a single 5 volt power supply.

LOGIC

The 8T14 contains three line receivers, each of which can be strobed independently. Additional logic is included to allow the output to be forced to a logic "0" by external control signals. (Refer to Figure 6 for complete logic diagram.)

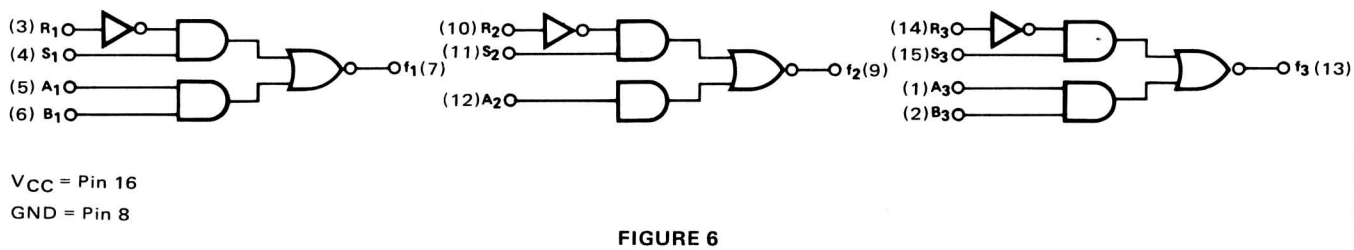


FIGURE 6

CIRCUIT DESCRIPTION

The receiver input of the 8T14 is basically a differential amplifier with a constant current source replacing the common emitter resistor (see Figure 7). The input impendance is therefore very large, being typically 30 – 50 kilohms. Loading effects are then minimal, an important factor when several receivers are used on the same transmission line.

The output of each line receiver is similar to that used in high speed TTL logic gates. Output rise time is reduced with the low impedance Darlington-type pull-up structure. Typical source and sink current capability over the full temperature range are shown in Figures 8 and 9.

1/3 8T14 LINE RECEIVER

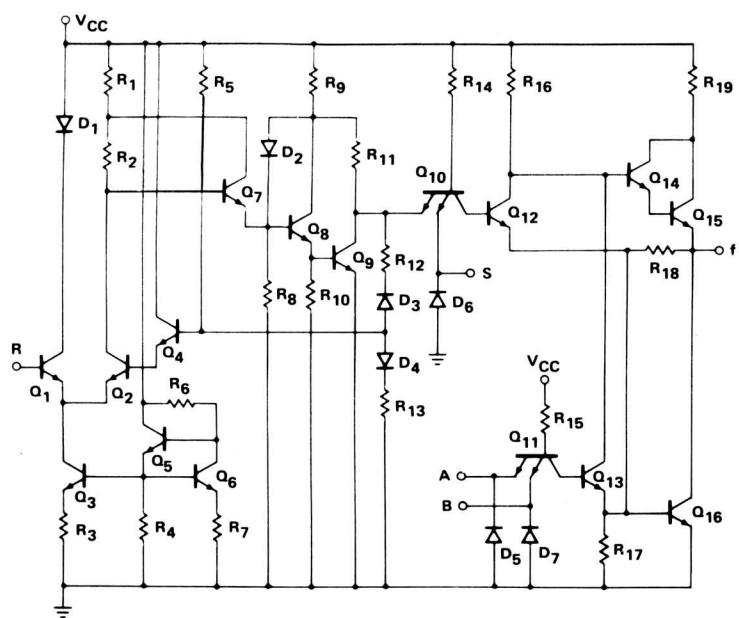


FIGURE 7

HYSTERESIS

The 8T14 exhibits typically 0.5 volt hysteresis as shown in Figure 10. Using the values of upper and lower threshold voltages as indicated, we can calculate the noise immunity for both logic one and zero levels. These calculations assume that the device is being driven with a logic swing of 0.4 to 2.8 volts.

Logic "1" Noise Immunity (N_1)

$$N_1 = V_1 - V_{UT} = 2.8V - 1.35V$$

$$N_1 = 1.45V$$

Logic "0" Noise Immunity (N_0)

$$N_0 = V_{LT} - V_0 = 1.85V - 0.4V$$

$$N_0 = 1.45V$$

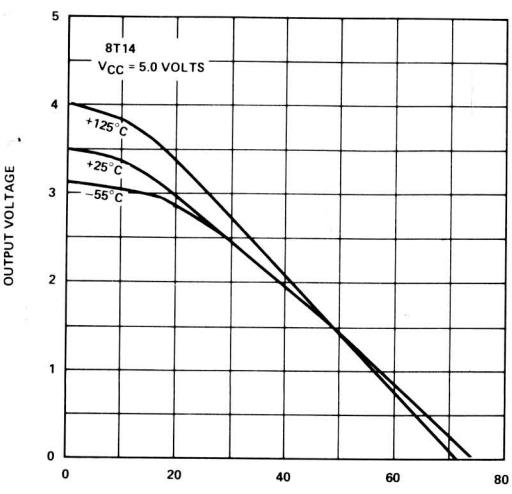


FIGURE 8

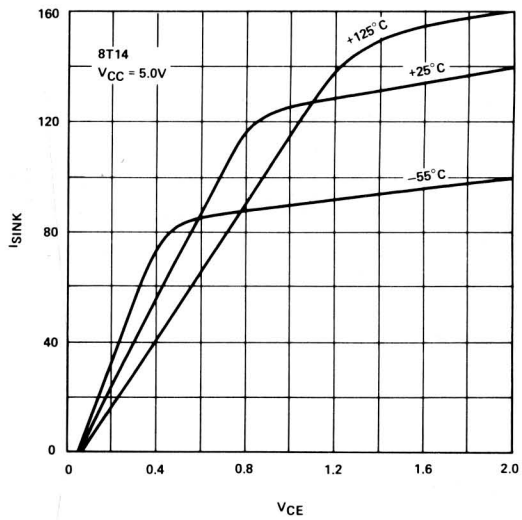


FIGURE 9

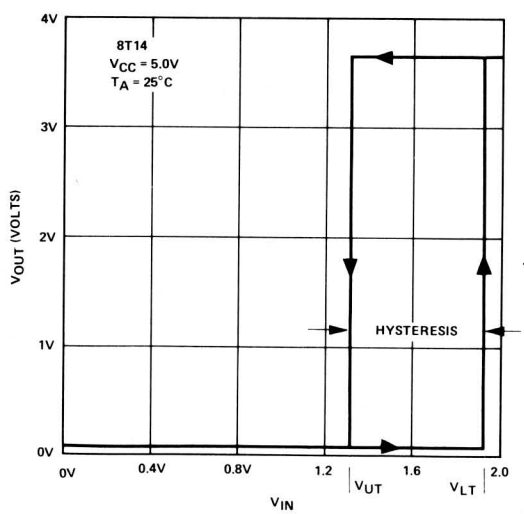
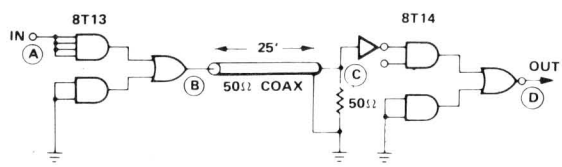


FIGURE 10

APPLICATIONS



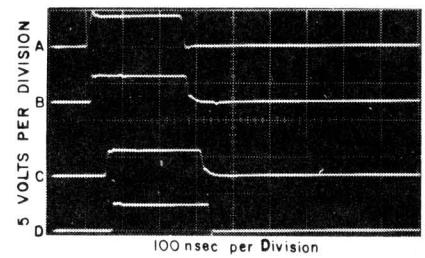
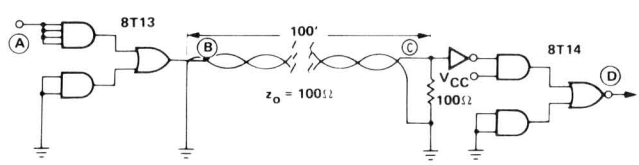


FIGURE 11

TWISTED PAIR



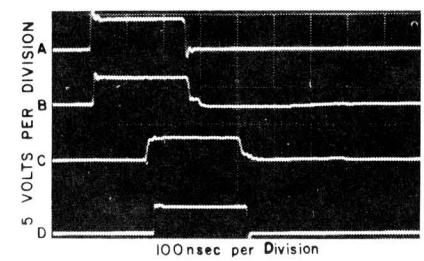
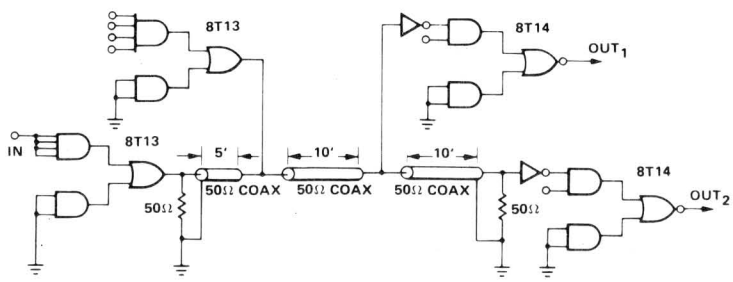


FIGURE 12

PARTY–LINE APPLICATION



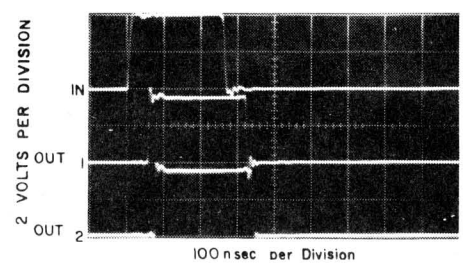


FIGURE 13

GENERAL EQUATIONS FOR PARTY LINE APPLICATIONS

When multiple drivers and receivers are tied onto a common bus in a party-line applications, it can be easily ascertained if the required current is within the drive capability of an 8T13 driver. Figure 14 shows a generalized example.

The equations given below will show if a driver can handle the load.

$$I_{OUT(1)}\Big|_{V_{OUT(1)} = 2.4V} \geq I_{TERMINATION} + I_{LOAD}$$

Where: $I_{LOAD} = (m - 1)\, I_{LEAK(1)} + n I_{IN(1)}$

m = number of drivers

n = number of receivers

Example:

Can the 8T13 and 8T14 be used in a bus-organized system where 15 drivers and 20 receivers are tied onto one common bus. The bus is 100Ω coax-cable, terminated at both ends.

Given: m = 15

n = 20

$R_{TERM} = 100\Omega$

$$I_{OUT(1)}\Big|_{\text{at } V_{OUT(1)} = 2.4V} = 75mA$$

$I_{OUT(1)_{LEAK}} = 500\mu A$

$I_{IN(1)} = 0.17mA$

$I_{LOAD} = (14)\ (0.5mA) + 20(0.17)mA$

$= 10.2mA$

$$I_{TERM} = \frac{2.4V}{50\Omega} = 48mA$$

$I_{TERM} + I_{LOAD} \leq I_{OUT(1)}$

$58.2mA < 75mA$

The answer shows that the above application is well within the 8T13's drive capability.

PARTY–LINE APPLICATION

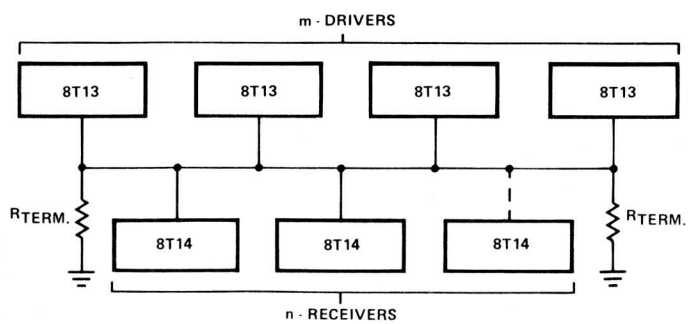


FIGURE 14

USING THE 8T14 AS A SCHMITT TRIGGER

The Signetics 8T14 Triple Line Receiver was designed primarily for data communication systems where digital information must be recovered with a high degree of accuracy, even in the presence of noise.

However, as shown in Figure 1, the Line Receiver inputs having hysteresis together with the additional logic functions available make the 8T14 a powerful multipurpose device. For a thorough discussion of the 8T14's electrical characteristics please refer to the applications memo covering the 8T13 Line Driver and the 8T14 Line Receiver.

8T14 TRIPLE LINE RECEIVER

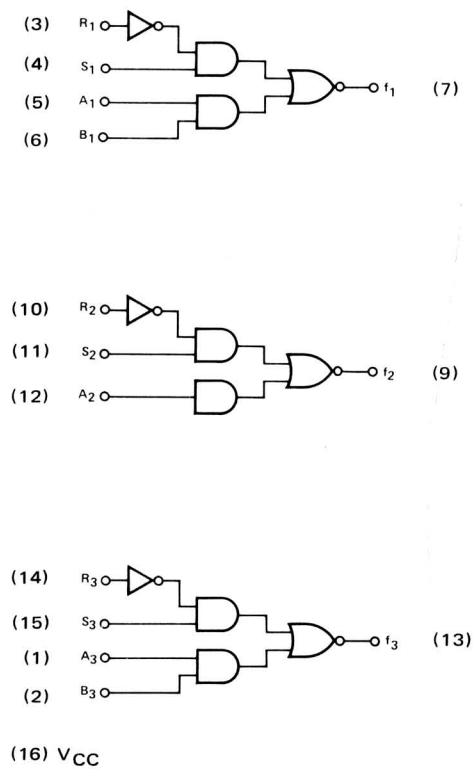


FIGURE 1

The built-in hysteresis of the line receiver makes it ideal for use as a Schmitt trigger. For example, signals with slow transition times can be reshaped with the 8T14 to be suitable for use with high speed logic as illustrated in Figure 2. By taking advantage of the additional logic inputs, the circuit could also be used as a controlled Schmitt trigger. Typical rise and fall times of the 8T14 are less than 10ns with minimum capacitive loading.

SCHMITT TRIGGER

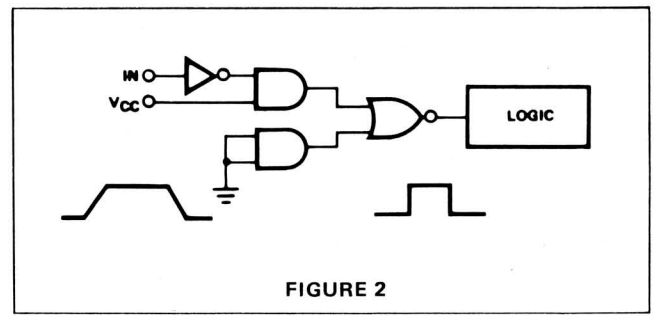


FIGURE 2

A special case of a Schmitt trigger application is sine-to-square wave conversion. The circuit shown in Figure 3 was found to be a very effective and convenient means of driving the frequency divider chain of a digital clock.

SINE–TO–SQUARE WAVE CONVERTER

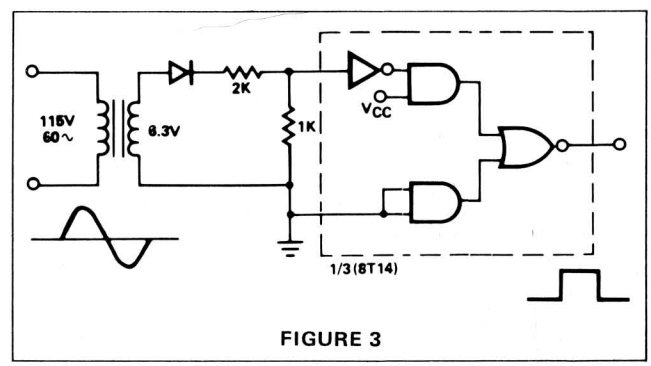


FIGURE 3

The Schmitt trigger characteristics of the 8T14 can also be used to advantage in a monostable multivibrator, or one-shot as illustrated in Figure 4.

ONE–SHOT

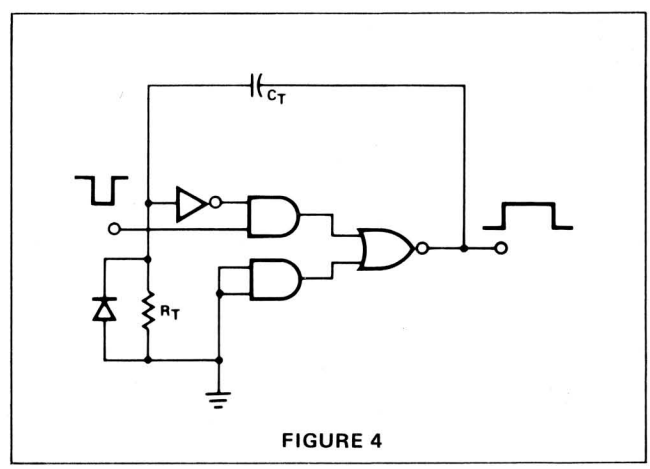


FIGURE 4

With resistor values less than 5K, the output pulse width is $\cong 0.9\ R_T\ C_T$. Above 5K, R_T begins to approach the input impedance of the 8T14 and the equation is no longer valid. Figure 5 is a graph of pulse width versus timing capacitance for the circut shown in Figure 4.

OUTPUT PULSE WIDTH VS. TIMING CAPACITANCE

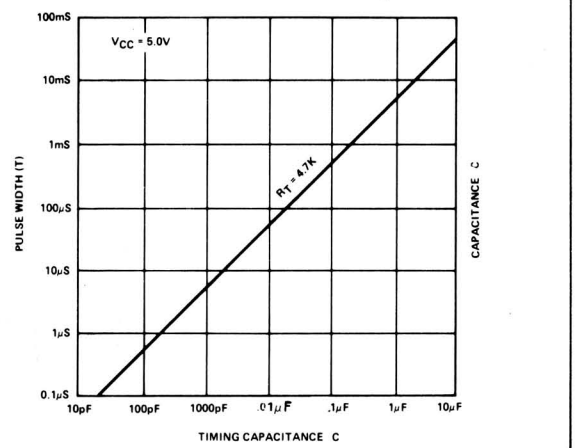


FIGURE 5

To increase pulse width, capacitor multiplication with PNP transistors can be used as indicated in Figure 6. The effective capacitance becomes approximately $\beta X C_T$. Using a 10KΩ resistor and 47μF capacitor, pulse widths of 50 seconds were obtained.

ONE SHOT WITH BETA MULTIPLIER

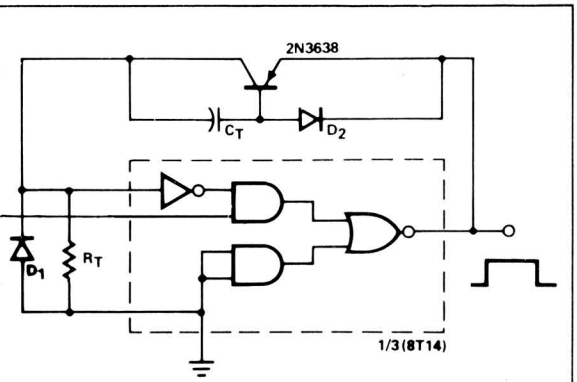


FIGURE 6

Without diode D_2, capacitor C_T does not discharge rapidly below 1.5 volts and does not allow the one-shot to retrigger. The diode provides a low impedance path back through the saturated output transistor and significantly increases the duty cycle.

When the input pulse width is larger than the required output pulse, the input can be differentiated by a small series capacitor. Using a 22pF capacitor, output pulse widths as short as 50ns can be obtained.

By providing an additional stage of inversion, the 8T14 can be used as a gated oscillator as shown in Figure 7. Using one of the remaining receivers in the package for the inverter the circuit was found to oscillate at:

$$f_{osc} \cong \frac{1}{0.7\ RC}$$

OSCILLATOR

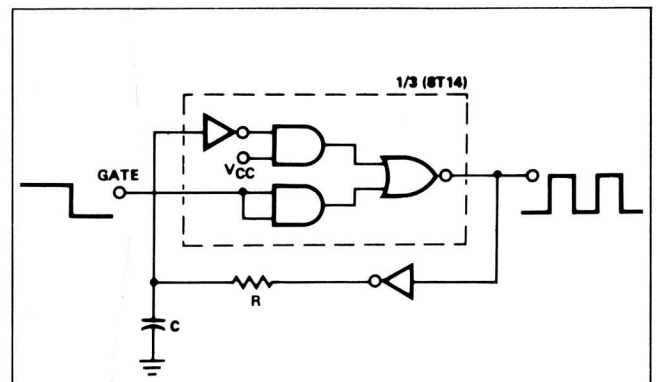


FIGURE 7

Figure 8 is a graph of oscillator frequency versus capacitance for two values of resistance. With the addition of a Hex Inverter such as Signetics 8890 three separate oscillators with buffered outputs could be built with only two packages.

OSCILLATOR FREQUENCY VS. CAPACITANCE

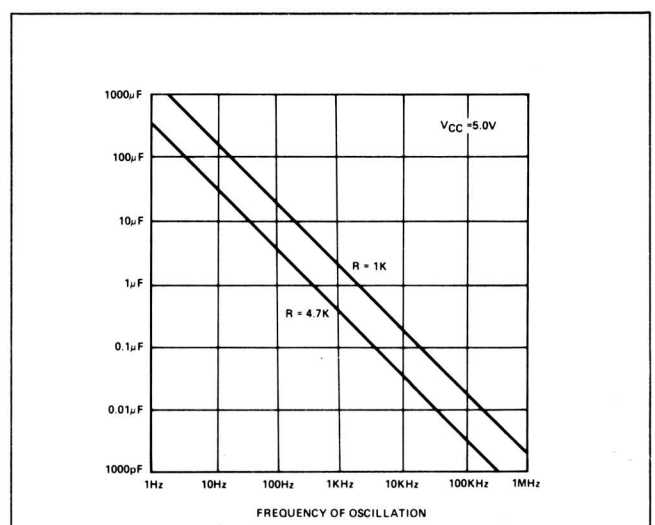


FIGURE 8

8T15 LINE DRIVER / 8T16 LINE RECEIVER

8T15 DUAL LINE DRIVER

The 8T15 Dual Communications Line Driver provides line Driving capability for data transmission between data communication and terminal equipment. The device meets or exceeds the requirements of EIA Standard RS-232B and C, MIL STD-188B and CCITT V 24.

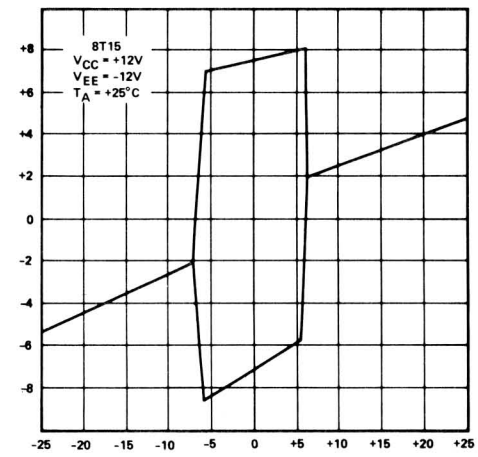
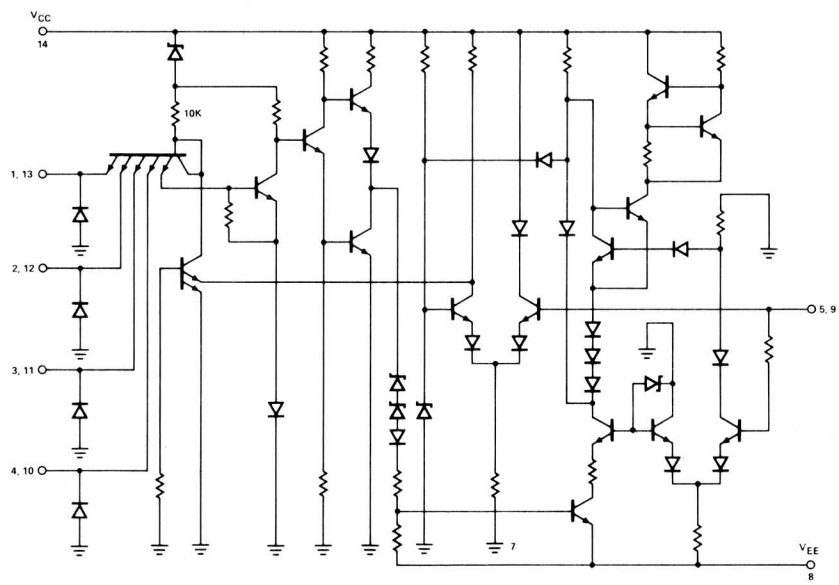


FIGURE 1

CIRCUIT DESCRIPTION

The 8T15 requires a dual power supply with nominal voltages of +12 and -12V volts. The output circuit features current limiting and can be shorted to ±25 volts without damage. Figure 1 shows the typical output characteristics for all possible operating conditions. Above approximately ±7 volts, the effects of current limiting cause the output impedance to increase to ⩾ 5 kilohms.

CIRCUIT SCHEMATIC



LOGIC DIAGRAM

As shown in Figure 2, each driver performs the logic NAND function of four inputs and will accept standard TTL logic levels. The output is buffered to drive interface lines with nominal data levels of +6V and -6V. Output slew rate may be adjusted by attaching and external capacitor from the output terminal to ground. The outputs are protected against damage caused by accidental shorting to as high as ±25 volts.

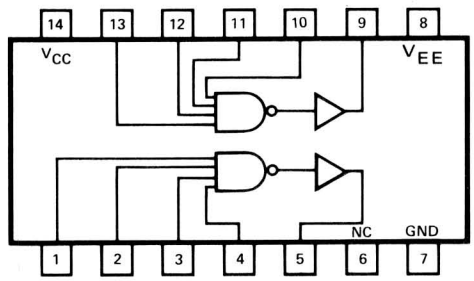


FIGURE 2

Figure 3 shows the typical transfer curve of the Line Driver at +25°C. Except for the output voltage swing of ±6 volts, the curve is essentially identical to that for a standard TTL gate.

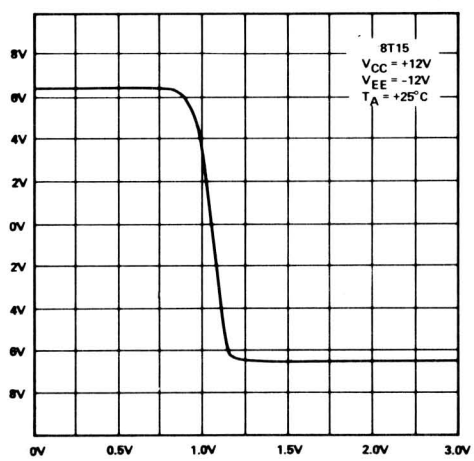
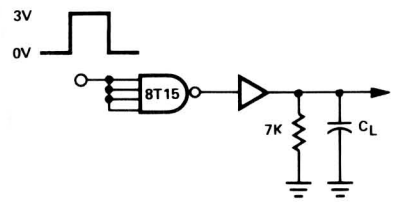
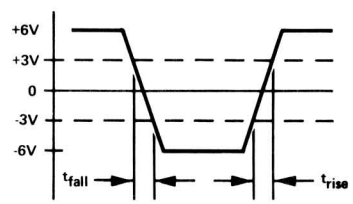


FIGURE 3

In systems where crosstalk is likely to occur between transmission lines, the rise and fall time of the data pulse can be tailored by connecting a capacitor from the output of the 8T15 to ground. Since the output current in either a "1" or "0" state is supplied through a constant current source, the transition time is a linear function of the load capacitance as shown in Figure 4. The circuit below was used to measure the transition time as C_L was varied between 0 and 1μf.





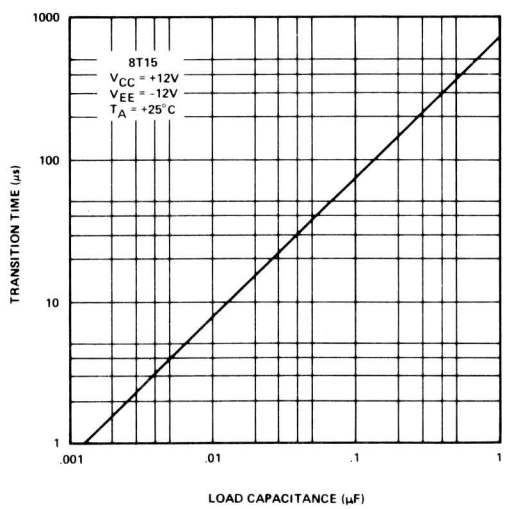


FIGURE 4

Table 1 provides a summary of the specific requirements of EIA Standard RS-232B and C, MIL STD-188B and CCITT V 24 for Communications Line Drivers along with the electrical characteristics of the Signetics 8T15.

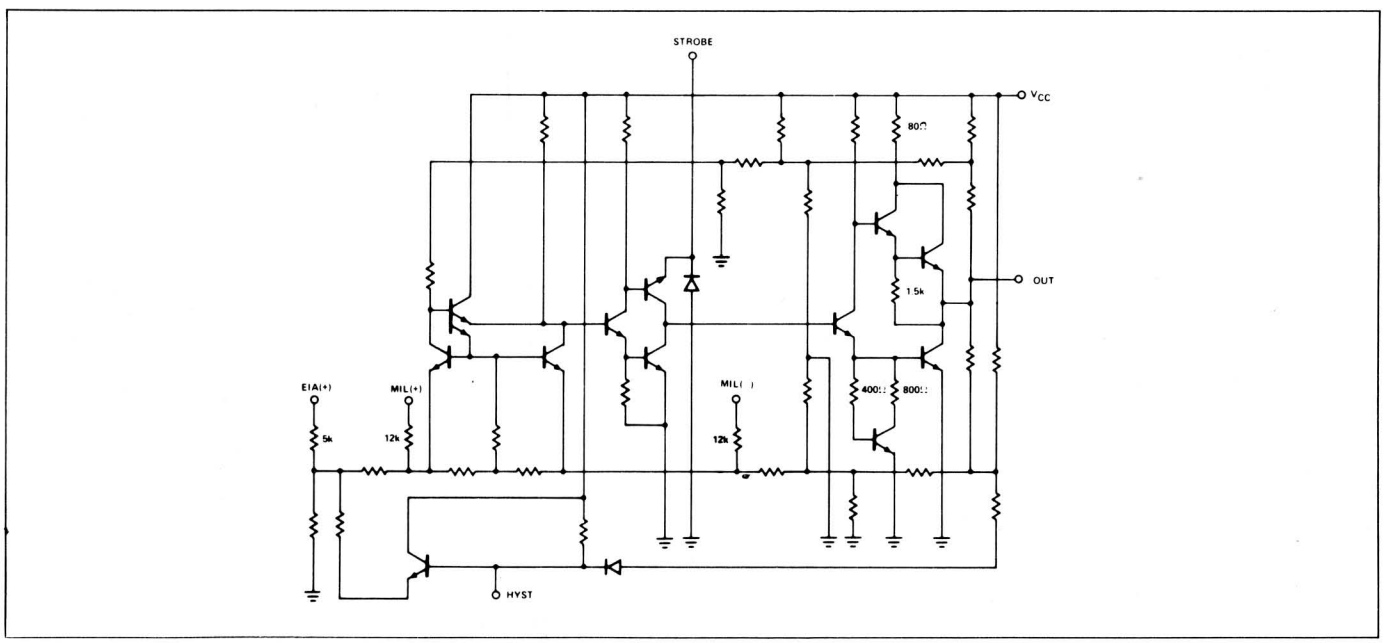
SPECIFICATION	EIA RS-232B, C	MIL-STD-188B	CCITT V24	SIGNETICS 8T15	
				(LIMIT)	(TYPICAL)
Output Voltage "1"	-5Vmin.(R_L = 3000Ω) -15Vmax.(R_L = 7000Ω)	-6 ±1V	-5Vmin. (R_L = 3000Ω) -15Vmax.(R_L = 7000Ω)	-5Vmin. -7Vmax at 4mA	-6V at 4mA
Output Voltage "0"	+5Vmin.(R_L = 3000Ω) +15Vmax.(R_L = 7000Ω)	+6 ±1V	+5Vmin.(R_L = 3000Ω) +15Vmax.(R_L = 7000Ω)	+5Vmin., 7Vmax. at -4mA	+6V at -4mA
Source Impedance (power on)	Not Specified	100Ω max. for I < 10mA	Not Specified		95Ω for ±(0.5 to 4.0 mA)
Source Impedance (power off)	300min. at ±2V	N/A	300min. at ±2V	300min. at ±2V	2.5MΩ
Max. Short Circuit Current	±500mA max. (to ±25V)	100mA max. (to ground)	±500mA max. (to ±25V)	±25mA max. (to ±25V)	±5mA (to ±25V)
Wave Shape (rise and fall time)	±4% of pulse Interval (max.)	±5% of pulse Interval (min.)		4μs-3000pF 200ns-20pF	2μs-3000pF 25ns-20pF
Bit Rate	0-20KHz	4KHz normal	20KHz max.		3MHz
Open Circuit Drive	±25V max.	±6V ±1V		±6V ±1V	±6V
Signal Characteristics	1ms max. transition		1ms max. transition		2μs with C_L = 3000pF
	30V/μs max. dV/dt		30V/μs max. dV/dt		20V/μs with C_L = 500pF

TABLE 1

8T16 DUAL LINE RECEIVER

The 8T16 was designed for use as either an EIA or MIL Line Receiver for interfacing with data communication and terminal equipment. Two MIL inputs (MIL+ and MIL-) and one EIA input are provided on each receiver. Each output can be strobed independently and a hysteresis control is provided for shifting the threshold voltages for use in the EIA Fail-Safe mode. The 8T16 operates from a single +5 volt power supply.

CIRCUIT SCHEMATIC



LOGIC DIAGRAM

The strobe input operates as follows:

a) A "0" on the strobe input allows data transfer.

b) A "1" on the strobe input holds the output high. (Throughout this Application Memo the negative logic convention is used, i.e., a logic "1" refers to a relative low voltage and a logic "0" to a relative high voltage.)

It is important to note that when using the EIA input both MIL inputs must be grounded. The EIA input can be left open when unused.

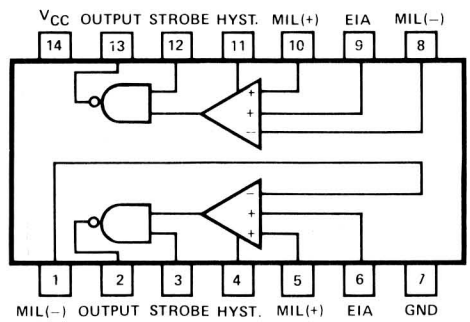


FIGURE 5

The 8T16 Line Receiver accepts single-ended (MIL and EIA) or, differential (MIL) signals and converts them to standard TTL logic levels. The circuit employs hysteresis to obtain the high noise margins required when the receivers must operate in noisy environments. The upper threshold voltage can be shifted above 0 volts by grounding the hysteresis control line. This allows the receiver to be used in the EIA Fail-Safe mode. Figures 6 through 8 illustrate typical hysteresis characteristics for all three operating conditions.

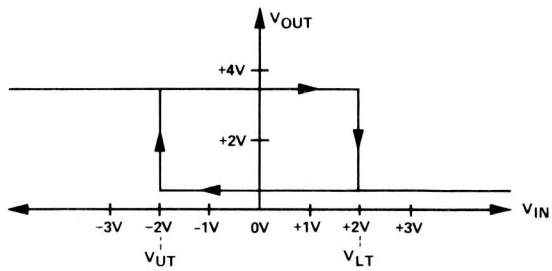


FIGURE 6

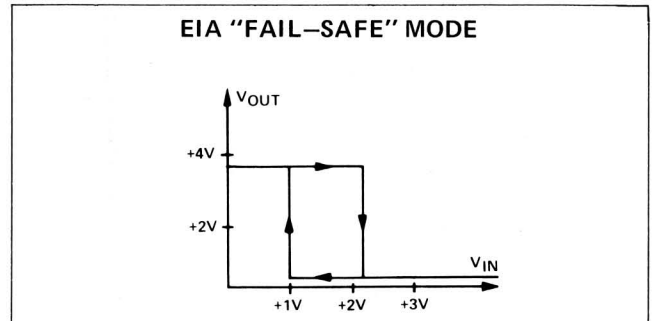


FIGURE 7

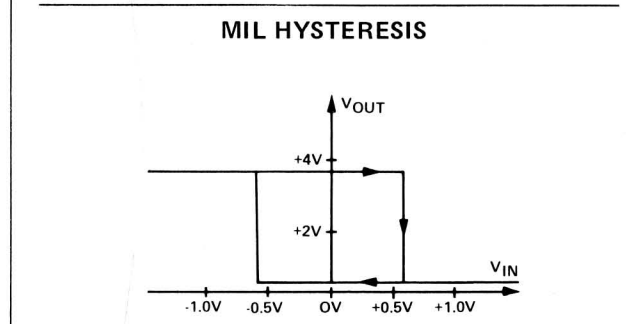


FIGURE 8

Figure 9 is a curve of noise immunity versus pulse width assuming the receiver is being driven with a signal whose amplitude is normally ±6 volts. The noise rejection capability of the 8T16 provides approximately 15 volts of noise immunity to pulses ⩾ 30ns.

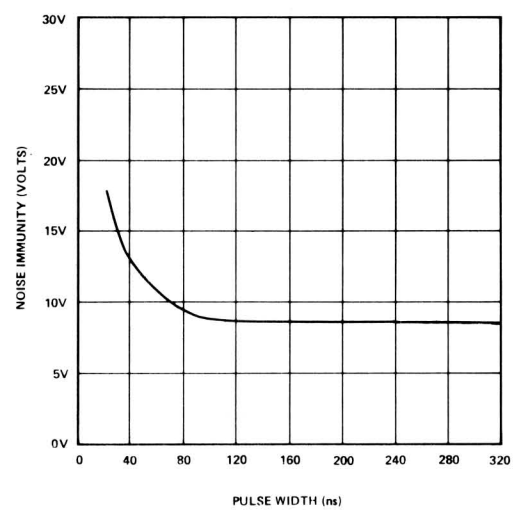


FIGURE 9

The 8T16 output is TTL compatible as shown in Figures 10 and 11 where the typical source and sink current capability are illustrated for the 0°C to +75°C temperature range.

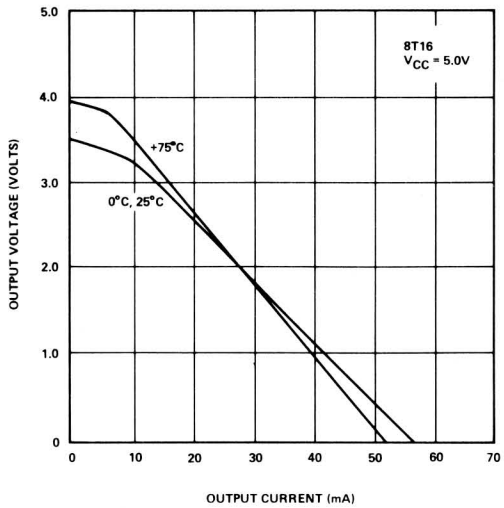


FIGURE 10

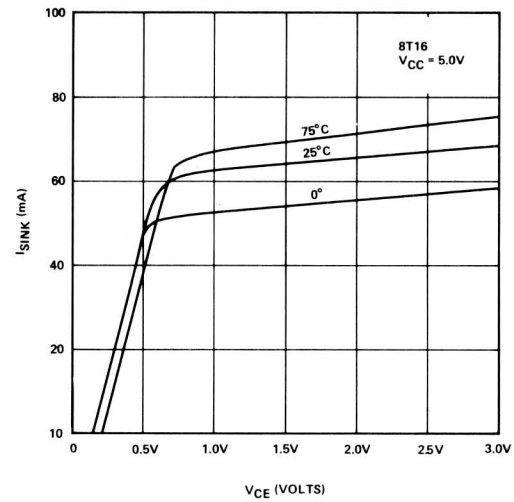


FIGURE 11

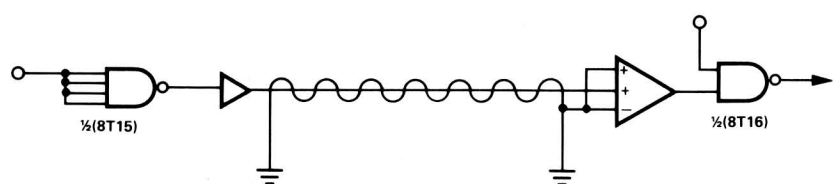
SPECIFICATION	EIA RS-232B, C	MIL-STD 188B	CCITT V24	SIGNETICS 8T16	
				LIMIT	TYPICAL
Input Thresholds (V) Max.	+3V, -3V	Not Specified	+3V, -3V	+3V, -3V (1) +0.9V, -0.9V (2) +3V, +0.3V (3)	+2V, -2V (1) +0.6V, -0.6V (2) +2.1V, +1V (3)
Input Thresholds (1) Max.	Not Specified	0.1mA max.	Not Specified	.1mA max.	0.050mA
Input Resistance	3K min., 7K max.	6K min.	3KΩ min., 7K max.	3K min. 7K max. (EIA) 7.5K min. (MIL)	5K (EIA) 12K (MIL)
Hysteresis	Not Specified	Not Specified	Not Specified	2.4V min. (EIA) 0.7V min (MIL)	4V (EIA) 1.2V (MIL)
Max. Input Voltage	±25V (min.)	Not Specified	±25V (min.)	+25V (EIA)	
V_{CC}	Not Specified	Not Specified	Not Specified	+7V	+5V ±5%

NOTES: 1) EIA Input, Hysteresis terminal open 2) MIL Input 3) EIA Input, Hysteresis terminal grounded

TABLE 2

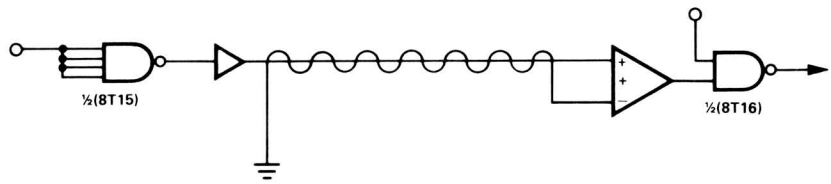
APPLICATIONS

HIGH DIFFERENTIAL NOISE IMMUNITY

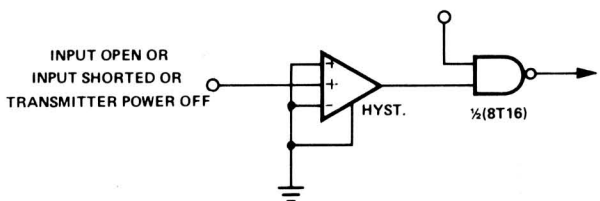


APPLICATIONS (Cont'd)

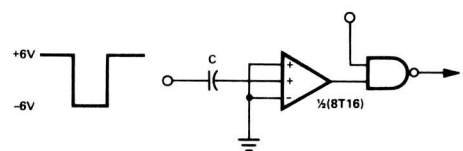
HIGH COMMON MODE NOISE IMMUNITY



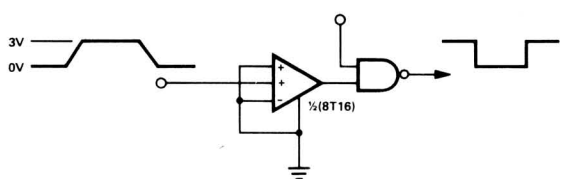
EIA FAIL-SAFE OPERATION



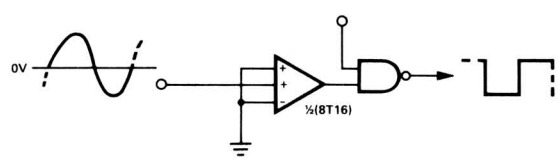
AC COUPLED OPERATION



SCHMITT TRIGGER



SINE-TO SQUARE WAVE CONVERTER



8T20 BI-DIRECTIONAL ONE-SHOT

INTRODUCTION

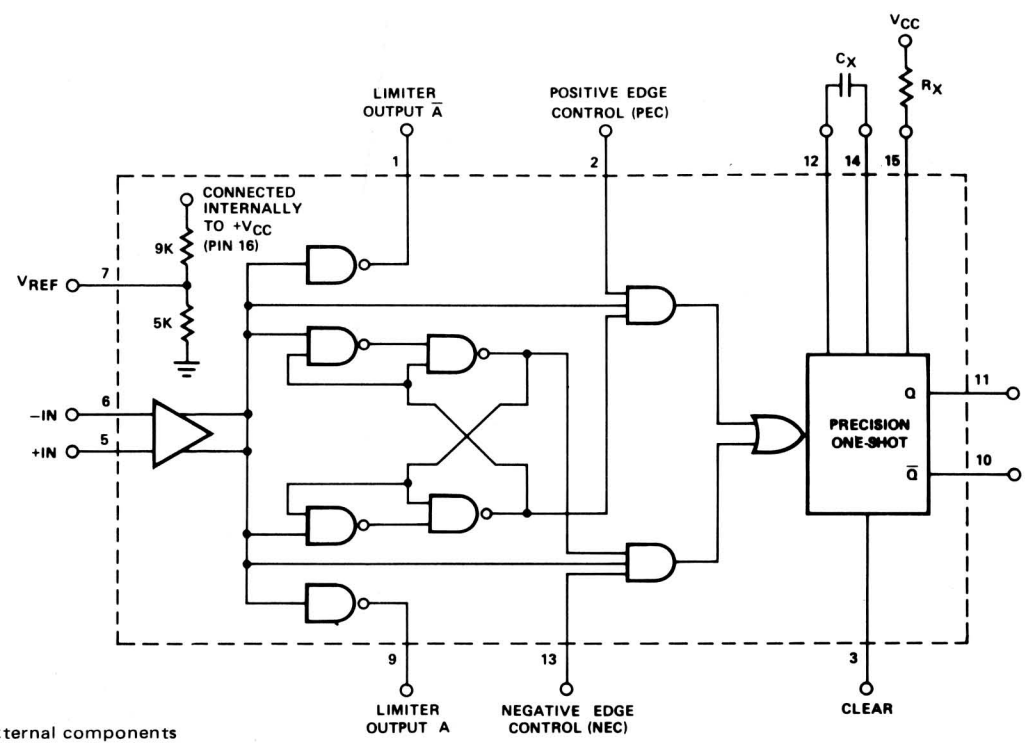
The 8T20 bidirectional one-shot is a functional building block that combines in one monolithic IC a high speed comparator, digital control circuitry and a precision one-shot. As shown in Figure I, the device may be driven with differential or single ended signals; and for convenience, a resistive divider on the chip will provide a TTL reference voltage. The comparator outputs are limited and made accessible through buffers for additional design flexibility. The output of the limiter feeds digital control circuitry which generates a trigger pulse each time the input makes a positive or negative transition across the reference level. By means of a positive edge control (PEC) as well as a negative edge control (NEC) the precision one-shot may be conditioned to trigger on the positive edge and/or the negative edge. The one-shot is non-retriggerable and its period may be adjusted by means of external timing components. An active-high clear input inhibits the operation of the 8T20 and terminates already initiated timing cycles as well.

The 8T20 will simplify system design and significantly reduce parts count in applications where signal conditioning and timing pulse generation is required. Input and output waveforms are shown in Figure 2 for easy reference. The usefulness of the 8T20 in magnetic recording of digital data and digital data transmission will be discussed among other applications.

DEVICE DESCRIPTION

The input stage of the 8T20 is a differential pair with high input sensitivity and a differential input impedance of approximately 2kΩ. The differential threshold voltage (V_T) is ±4mV maximum and is defined as the maximum offset voltage from the reference level of one input beyond which the one-shot is guaranteed to fire. Thus, by observing the first accessible digital output of the one-shot which is pin 12 (one of the C_X terminals), the DC input voltage (V_T) required to make the one-shot trigger can be ascertained.

LOGIC DIAGRAM



NOTES:
1. R_X,C_X external components
2. Pulsewidth $t_W = R_X C_X \text{Log}_e 2$
3. 4 V_{EE} = –5V ± 5%
4. 8 GND
5. 16 V_{CC} = +5V ± 5%

FIGURE 1

Common mode signals will not cause false triggering of the 8T20 as long as they are confined within the dynamic range of the analog inputs which is between -3.2V and +4.2V. Since in many applications TTL compatible signals are available to drive the 8T20, the output of an internal resistive divider can be connected to one of the differential inputs as a TTL threshold reference (approximately 1.6V).

The differential pair is followed by a level shifter and limiter circuit; but for simplicity, only the block diagram is shown in Figure 1. The comparator has differential outputs which feed the internal digital circuitry and for additional versatility they are also buffered and brought out (pins 1 and 9).

INPUT/OUTPUT WAVEFORMS

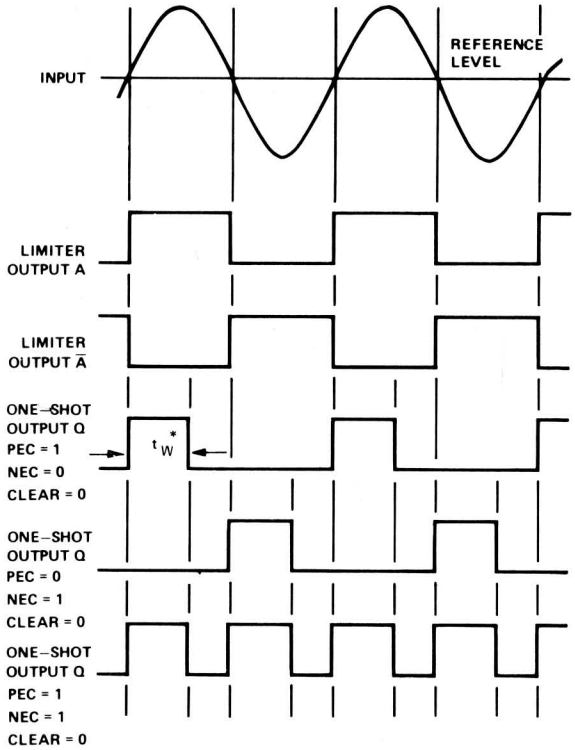


FIGURE 2

The input signal transitions which have been shaped by the limiter output of the comparator are processed by the pulse generating and control circuitry as shown in Figure 3. Input transitions at gates A and B are transformed into trigger pulses and the outputs C and D may be inhibited by means of the PEC and NEC signal. Thus the one-shot that follows the OR-gate E can trigger on either edge or both.

INTERNAL PULSE GENERATING AND CONTROL CIRCUITRY

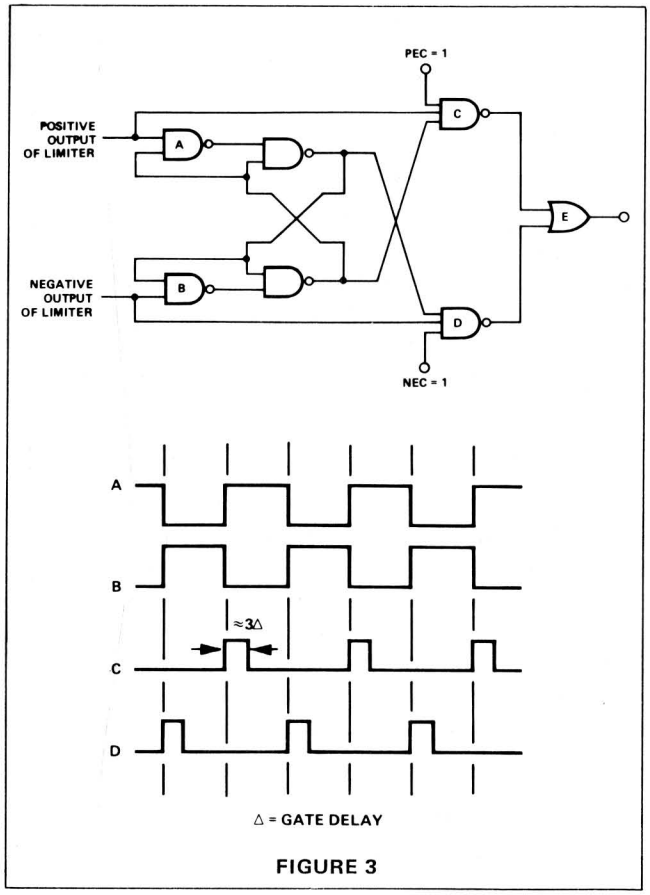


FIGURE 3

A simplified circuit diagram of the 8T20 timing circuit is shown in Figure 4. The design offers extremely accurate output pulse widths that depend essentially only on the accuracy of external timing components. The timing capacitor C_X can be charged rapidly through the emitter follower action of Q_2 permitting duty cycles in excess of 90%.

TIMING CIRCUIT

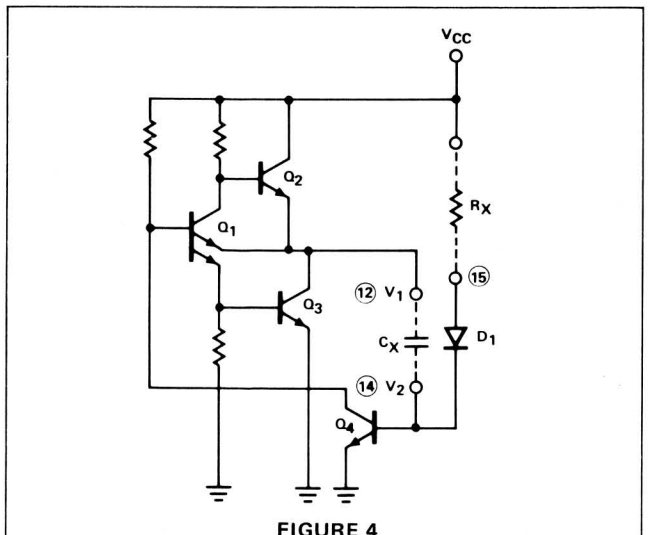


FIGURE 4

In the stable state, the capacitor is charged up to V_{CC} - V_{BEQ2} - V_{BEQ4}. When the one-shot is fired, Q_3 will turn on, clamping the capacitor C_X at V_{BEQ3}. As shown in the timing waveform, Figure 5, voltage V_2 drops from V_{BEQ4} to - V_{CC} + V_{BEQ2} + V_{BEQ3} + V_{BEQ4}. In this quasi-stable state C_X will charge through the timing resistor R_X towards V_{CC} - V_{D1}. When V_{BEQ4} is reached again, the one shot will revert to its stable state, only utilizing the linear part of the charging curve.

TIMING WAVEFORM FOR SIMPLIFIED ONE–SHOT

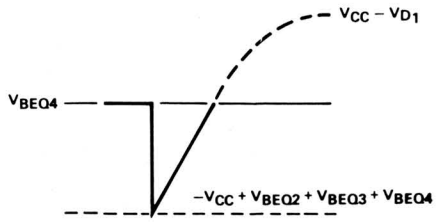


FIGURE 5

The output pulse width (t_W) can thus be calculated by setting $V_2 = V_{BEQ4}$ at $t = t_W$, resulting in:

$$e^{-t_W/R_XC_X} = \frac{-V_{CC} + V_{BEQ4} + V_{D1}}{-2V_{CC} + V_{BEQ2} + V_{BEQ3} + V_{BEQ4} + V_{D1}}$$

By close matching of the forward voltages of the diodes, pulse width (t_W) becomes:

$$t_W = R_XC_X \log_e 2 \doteq 0.69\ R_XC_X$$

Where:

t = sec
R = ohms
C = Farads

Stability over temperature and V_{CC} variations is better than ±1% and typical timing charts are shown in Figures 6 and 7. The timing resistor R_X should be restricted between 2kΩ on the lower end to get reasonable duty cycles and 40kΩ on the high end such that Q4 can still be turned on at low temperatures. C_X should not exceed 1000μF such that safe current levels are maintained in the recovery transistor Q2.

OUTPUT PULSEWIDTH VS. TIMING RESISTOR VALUE

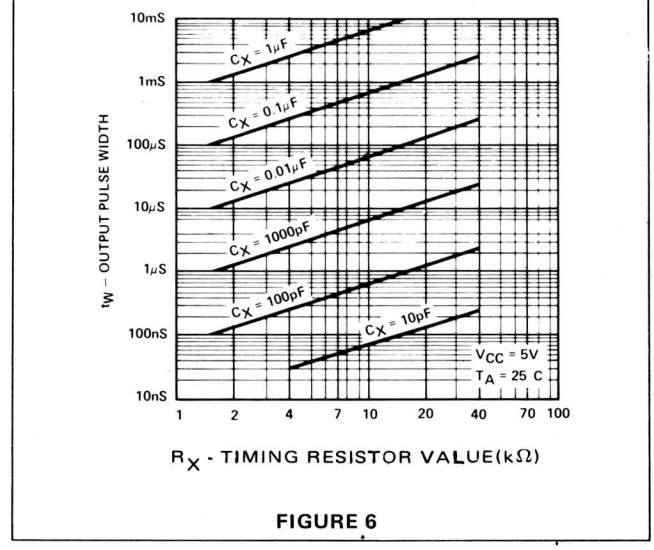


FIGURE 6

OUTPUT PULSEWIDTH VS. TIMING CAPACITOR VALUE

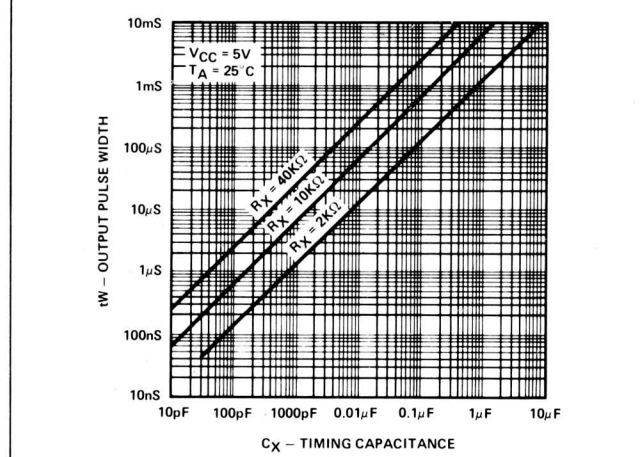


FIGURE 7

EXTENDING THE ONE–SHOT RANGE WITH A BETA–MULTIPLIER CIRCUIT

By adding an external transistor, the pulse width of the one-shot may be extended since very large timing resistors can be used as shown. However, it is more difficult to match V_{BE}'s and PW accuracy suffers slightly. In the connection shown in Figure 8, the internal diode is not utilized and the pulse width is calculated as follows:

$$e^{-t_W/R_XC_X} = \frac{-V_{CC} + V_{BEQ4} + V_{BEQX}}{-2V_{CC} + V_{BEQ2} + V_{BEQ3} + V_{BEQ4} + V_{BEQX}}$$

Thus, it can be seen that pulse width (t_W) will reduce again to

$$t_W = R_XC_X \log_e 2 = 0.69\ R_XC_X$$

if V_{BE} of the external transistor Q_X matches and tracks the internal transistor V_{BE}s. This somewhat surprising result is possible since C_X, connected as shown in Figure 8, will now charge towards V_{CC} instead of $V_{CC}-V_{D1}$ and V_2 is equal to $V_{BEQ4} + V_{BEQX}$ in the stable state of the one-shot.

For transistors with β = 100 timing resistor values up to 3.3MΩ can be used which combined with a 1000μF capacitor will give a pulse width t_W of approximately 35 min.

BETA MULTIPLIER CIRCUIT TO EXTEND PULSEWIDTH

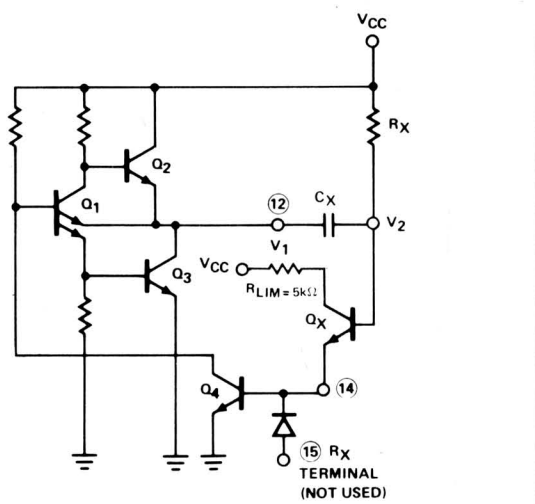


FIGURE 8

PULSE POSITION ERROR

In applications such as frequency doubling and processing of self-clocking digital codes received from magnetic media, it is extremely important to have minimum pulse position variations. As shown in Figure 9, when triggering on a positive transition a time delay Δt_1 is encountered, whereas on a negative transition a time delay Δt_2 is seen. A pulse position error (P.P.E.) can now be defined as P.P.E. = $|\Delta t_1 - \Delta t_2|$. Because of the close matching of components on the 8T20 chip, this error is typically less than 3ns, far superior to discrete implementations of this circuit.

DEFINITION OF PULSE POSITION ERROR

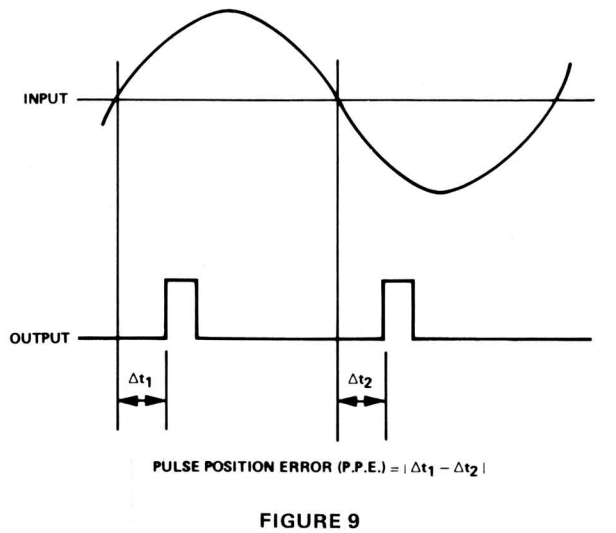


FIGURE 9

APPLICATION OF THE 8T20 IN DISC, DRUM AND TAPE PLAYBACK SYSTEMS

The 8T20 has been specifically designed for use in playback systems when recovering high-speed data from magnetic recording media. Because of the 8T20's inherent capability to double an incoming frequency with a low pulse position error (typ. < 3 ns) the device is particularly suited to process data encoded in self clocking formats such as those depicted in Figure 10. For clarity, these codes are referenced to the original clock.

Both the Manchester code and the double-frequency (diphase) code have at least one transition per bit cell, thus always containing clock information even with long strings of "1"s or "0"s. Manchester coding contains information in the direction of change, whereas double-frequency coding has two transitions per bit cell for a logical "1" and one transition per bit cell for a logical "0".

To recover a self-clocking code from magnetic media such as tape, disc or drum memories the 8T20 is used as illustrated in Figure 11. When data is read, the bits are sensed by the read-head as flux reversals to produce a waveform similar to the one which wrote the bits. Because of the low levels encontered, a pre-amplifier is necessary. The Signetics 592* pre-amplifier can be used for this purpose as a fixed gain (X 100 or X 400) or as an AGC amplifier without need for frequency compensation.

The information that is contained in the flux transitions of the original recording is shifted 90° in phase during playback. Flux transitions therefore, become peaks and differentiation is necessary to recover the phase of the write signal. Differentiation may be done within the 592 since each input transistor of the 592 has its own current source.

*See Signetics 592 Data Sheet.

As an alternate solution, the 592 may be followed by a differentiator as shown in Figure 11. The low pass-filter also indicated is necessary to limit high frequency noise.

The 8T20 input stage will act as a high gain limiter, squaring the pre-amplified and filtered signal. The device's digital pulse generating circuitry will detect positive and negative transitions (zero-crossings) that will trigger the internal one-shot as conditioned by the PEC and NEC control signals. A pulse train will result that contains the original data and clock information. This information is usually put on the read-bus for processing by pulse recognition circuitry to recover the data. It is customary in a high-precision system to use a phase-locked loop system to recover the original clock.

PHASE ENCODED DATA

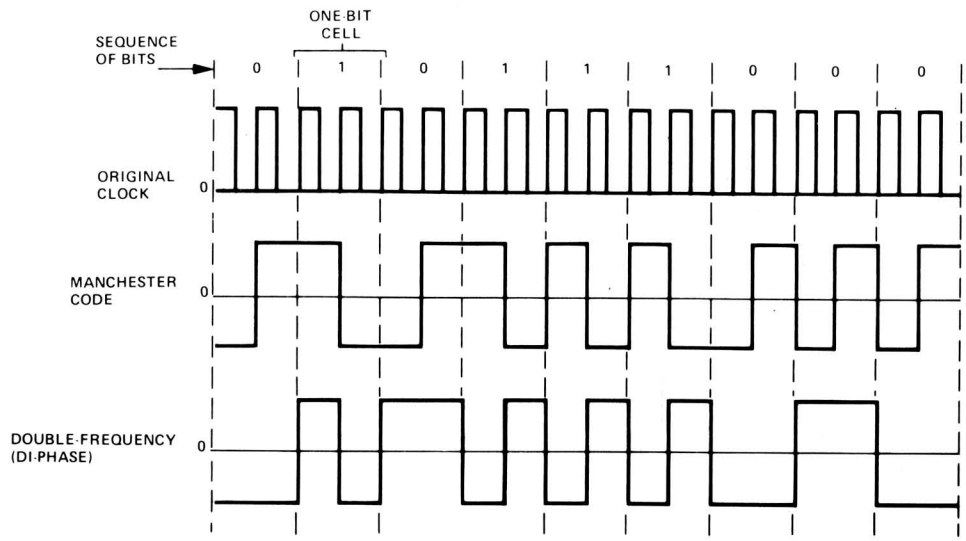


FIGURE 10

TYPICAL PHASE ENCODED PLAYBACK SYSTEM

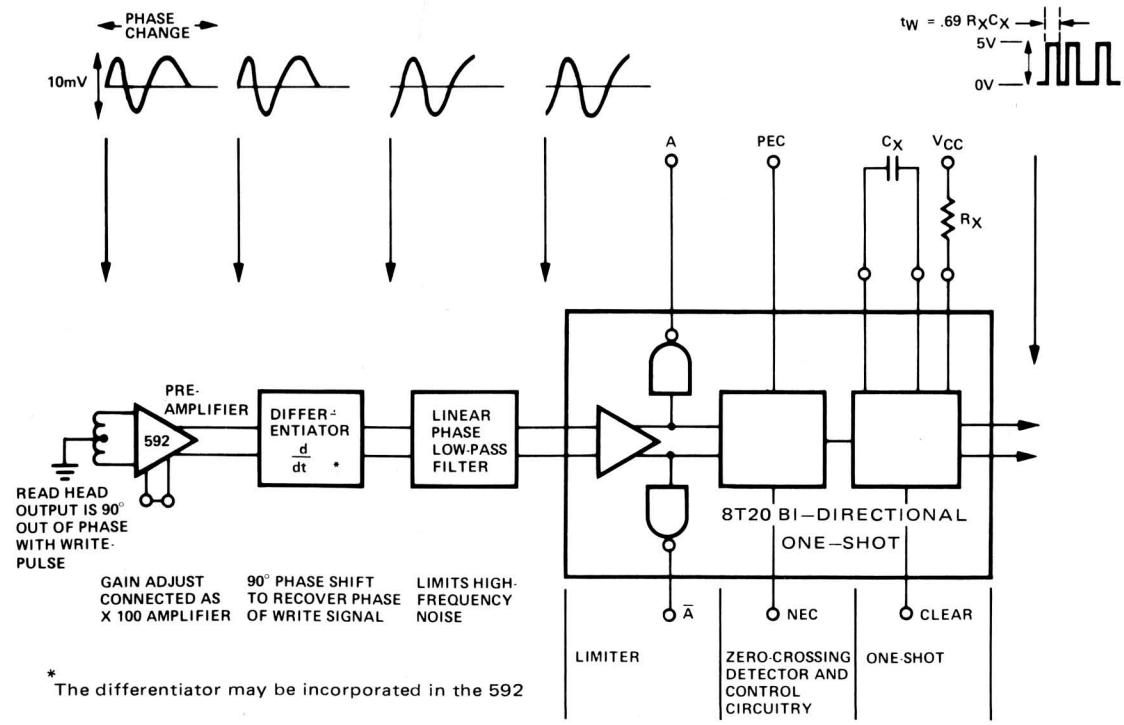


FIGURE 11

BINARY TO DI–PHASE TRANSMITTER

In airborne applications and systems where it is desirable to transmit data and clock information over the same transmission link the 8T20 is extremely useful. The waveforms in Figure 12 show that in order to convert binary data to a di-phase code it is necessary to conditionally double the input clock frequency, depending on whether a logical "1" or logical "0" is to be sent. The 8T20 is ideally suited for this frequency doubler application and far superior to exclusive-OR doubler circuits which suffer from pulse jitter problems. Because the 8T20 has triggering edge control, logic design is simplified over a discrete approach. The binary data can be fed into the NEC terminal without additional logic. The $\overline{Q}$ output of the bidirectional one-shot generates trigger pulses for the driver flip-flop (1/2 7473) as illustrated in Figure 13. To make the transmitter more useful, Figure 13 also shows how 10 channnels can be multiplexed by using an 8274 10-bit parallel-in, serial-out shift register and a 74192 divide-by-ten counter.

WAVEFORMS

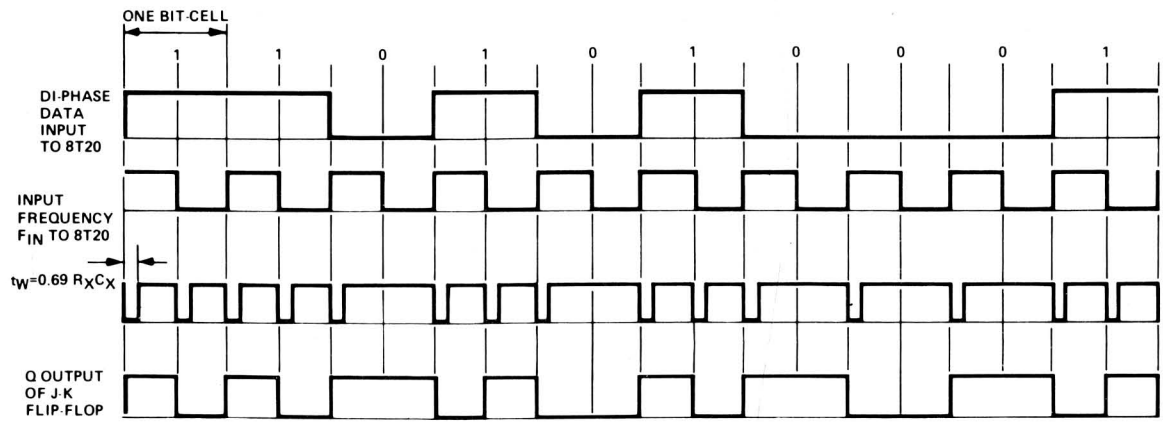


FIGURE 12

BINARY TO DI–PHASE TRANSMITTER

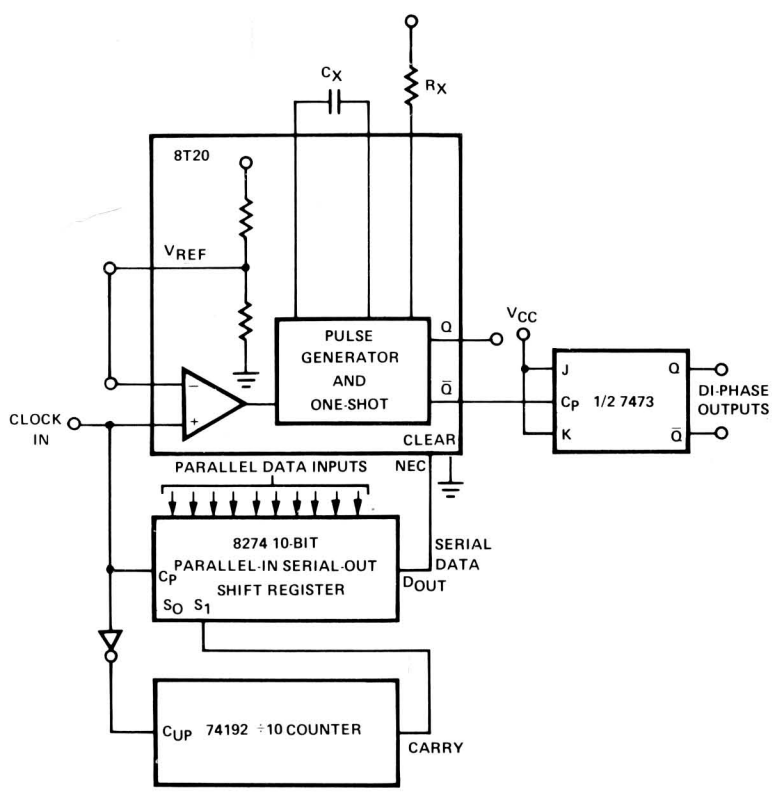


FIGURE 13

DI–PHASE TO BINARY RECEIVER

To recover the di-phase signal just described, Figure 14 shows the 8T20 input acting as a line receiver while the one-shot portion is conditioned as a frequency doubler. The addition of a 74121 non-retriggerable one-shot will recover the clock signal by choosing a duty cycle long enough to only permit one clock pulse per bit cell.

The 8T20 also triggers a 7473 flip-flop which is reset by the data-clock as well. Thus, whenever a logical "1" is to be clocked into the 8273 10-bit serial-in, parallel-out shift register, the Q output of the 7473 puts out a pulse. Figure 15 illustrates the waveforms associated with the di-phase to binary receiver circuit. The recovered data can be monitored at the Q_1 output of the 8273 shift register and is shown in Figure 14.

DI–PHASE TO BINARY RECEIVER

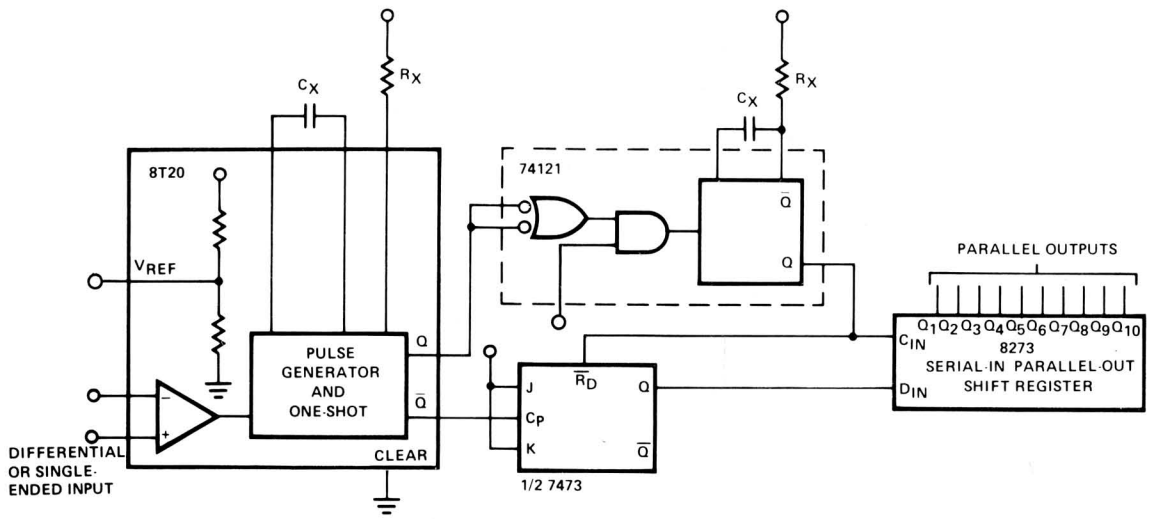


FIGURE 14

WAVEFORMS

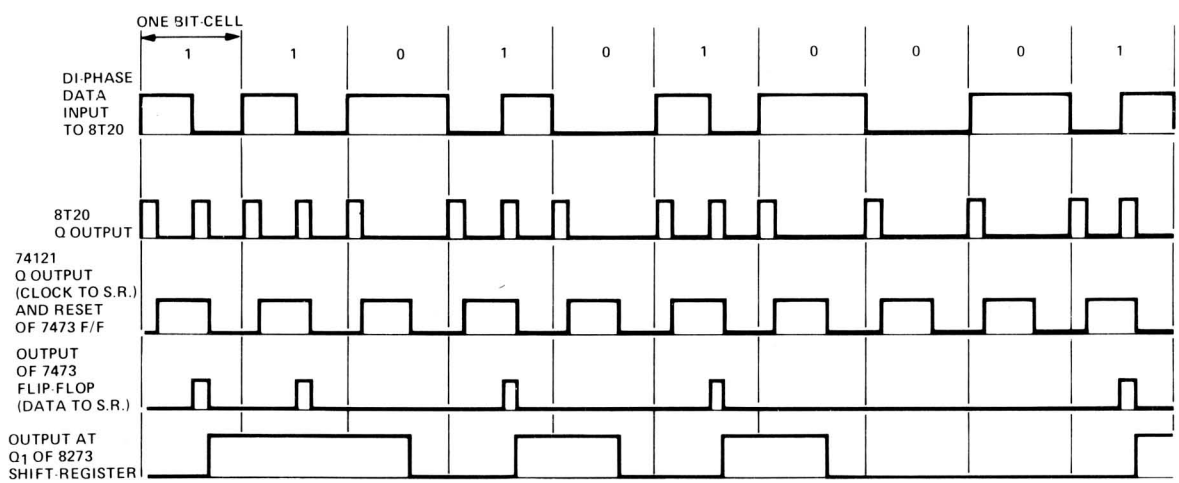


FIGURE 15

LINE RECEIVER WITH HYSTERESIS

The 8T20 can be conditioned to exhibit hysteresis when receiving signals from a high noise environment. As illustrated in Figure 16, one of the digital outputs of the limiter can be used to provide feedback to the signal input. By adding 3 resistors and a diode, upper and lower thresholds can be calculated as shown:

Lower threshold voltage:

$$V_{LT} = \frac{R_2}{R_1 + R_2} V_{CC}$$

Upper threshold voltage:

$$V_{UT} = \frac{R_2 \parallel R_3}{R_1 + R_2 \parallel R_3}$$

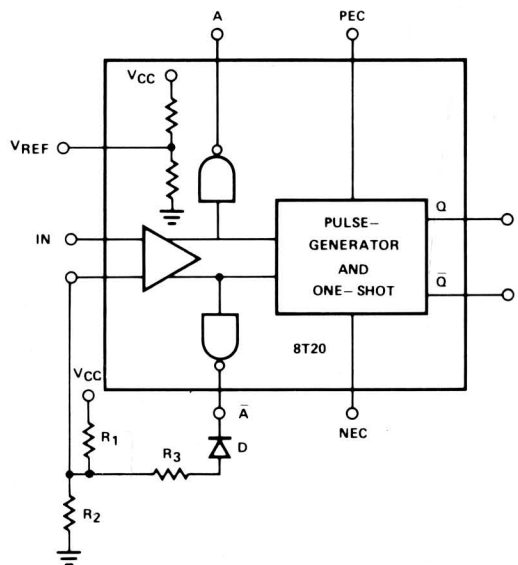
for R_1 = 7.5k, R_2 = 5.0k, R_3 = 5.0k and V_{CC} = 5.0V we get the following results:

$$V_{LT} \doteq 2.0V$$

$$V_{UT} \doteq 1.25V$$

Note that the resistors for the internal TTL reference in addition to one external resistor and a diode may be used for hysteresis purposes as well and V_{Ts} may be calculated as above.

LINE RECEIVER WITH HYSTERESIS



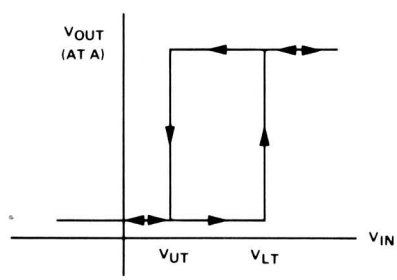


FIGURE 16

8T23 LINE DRIVER/8T24 LINE RECEIVER

INTRODUCTION

The 8T23 Dual Line Driver and 8T24 Triple Line Receiver have been designed to meet the IBM System 360 channel to control (I/O) interface specifications. These monolithic interface IC s are particularly useful to computer and peripheral equipment manufacturers who must interface with IBM computers and IBM compatible equipment.

The 8T23 and 8T24 are similar to the 8T13 Line Driver and 8T14 Line Receiver in their respective circuit designs and electrical characteristics. Therefore, the reader is referred to the applications memo covering the 8T13 and 8T14 for detailed circuit descriptions and more information pertaining to driving low impedance lines.

In the following discussion, IBM specifications (file No. S360-19) for interface circuits will be compared to the 8T23 and 8T24 electrical characteristics and their systems behavior.

DEVICE DESCRIPTION OF THE 8T23

As shown in Figure 1, the 8T23 consists of two line drivers that each have AND-OR logic to determine the output state of the driver. Both input and output are TTL compatible and the device is operated from a single 5V power supply. The outputs are uncommitted emitter followers with built-in short circuit protection and are capable of driving low impedance transmission lines such as coaxial cable, twisted pair or ribbon conductors. Outputs of 8T23 drivers may be dot-ORed for party-line applications as well as increased drive capability. For reference the typical output current vs. output voltage curve is shown in Fig. 2.

8T23 DUAL LINE DRIVER

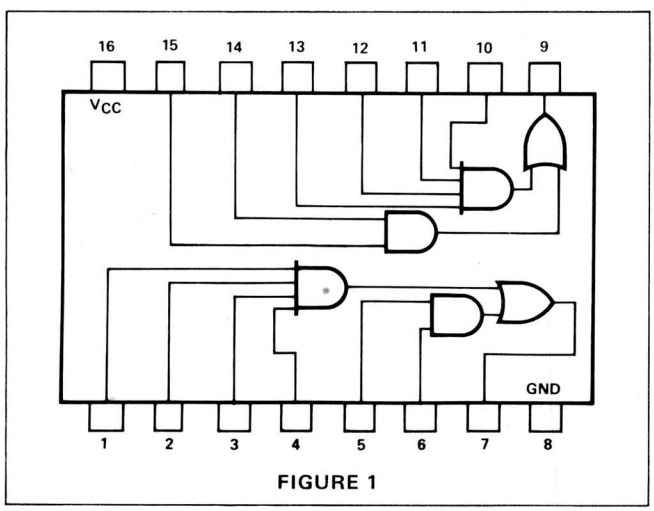


FIGURE 1

TYPICAL OUTPUT CURRENT VS. OUTPUT VOLTAGE FOR THE 8T23

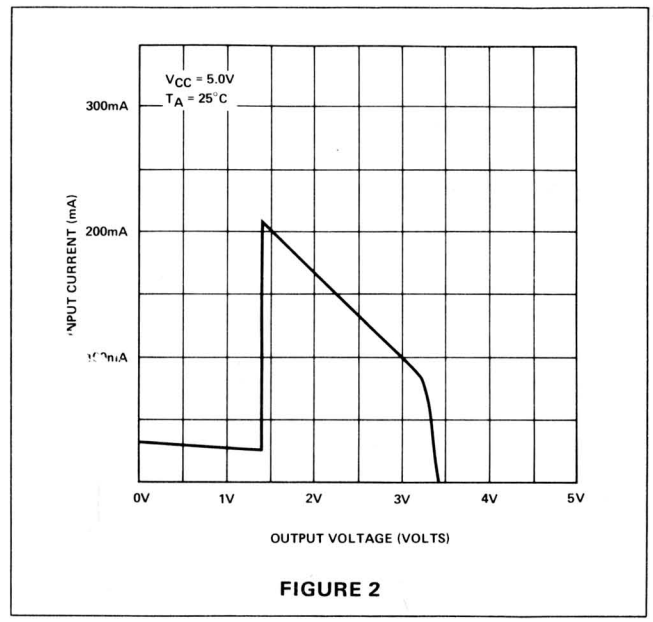


FIGURE 2

LINE DRIVER REQUIREMENTS

In Table I, the general electrical characteristics for the 8T23 line driver are compared to the requirement of the IBM specifications. It can be seen that the logical "1" and "0" level as well as fan-out considerations are met.

Because the 8T23 has uncommitted emitter follower outputs, multiple drivers and receivers can be connected onto one line in party-line applications. As required by the IBM specification, one driver can fan-out to ten receivers and up to ten driver outputs can be connected together (dot-ORed) to drive one receiver.

POWER–UP POWER–DOWN SEQUENCE FOR THE 8T23

The 8T23 line driver has been designed to ensure that no spurious noise is generated during a normal power-up or power-down sequence. Figures 3a and 3b show that the driver output stays in the logical "0" state regardless of the rate of rise or fall of V_{CC}, provided one or more inputs to each AND gate are at a logical "0" during the turn-on or turn-off of the power supply.

Figures 3c and 3d are included for completeness and show the results if a driver is powered-up with a logical "1" state defined at the output. The output will simply follow V_{CC} and not introduce noise.

LINE DRIVER

INTERFACE REQUIREMENT	IBM SPECIFICATION	8T23 SPECIFICATION	MEETS OR EXCEEDS IBM SPECIFICATION
$V_{OUT}(0)$ LOGICAL 0 OUTPUT VOLTAGE AT +240μA*	0.15V(MAX.)	0.15V(MAX.)	YES
$V_{OUT}(1)$ LOGICAL 1 OUTPUT VOLTAGE AT +59.3mA*	3.11V(MIN.)	3.11V(MIN.)	YES
FAN–OUT CAPABILITY	10 RECEIVERS	> 10 RECEIVERS	YES
DOT–OR CAPABILITY	10 DRIVERS	> 10 DRIVERS	YES

* Positive direction of current is out of the driver.

POWER–UP AND POWER–DOWN CHARACTERISTICS OF THE 8T23

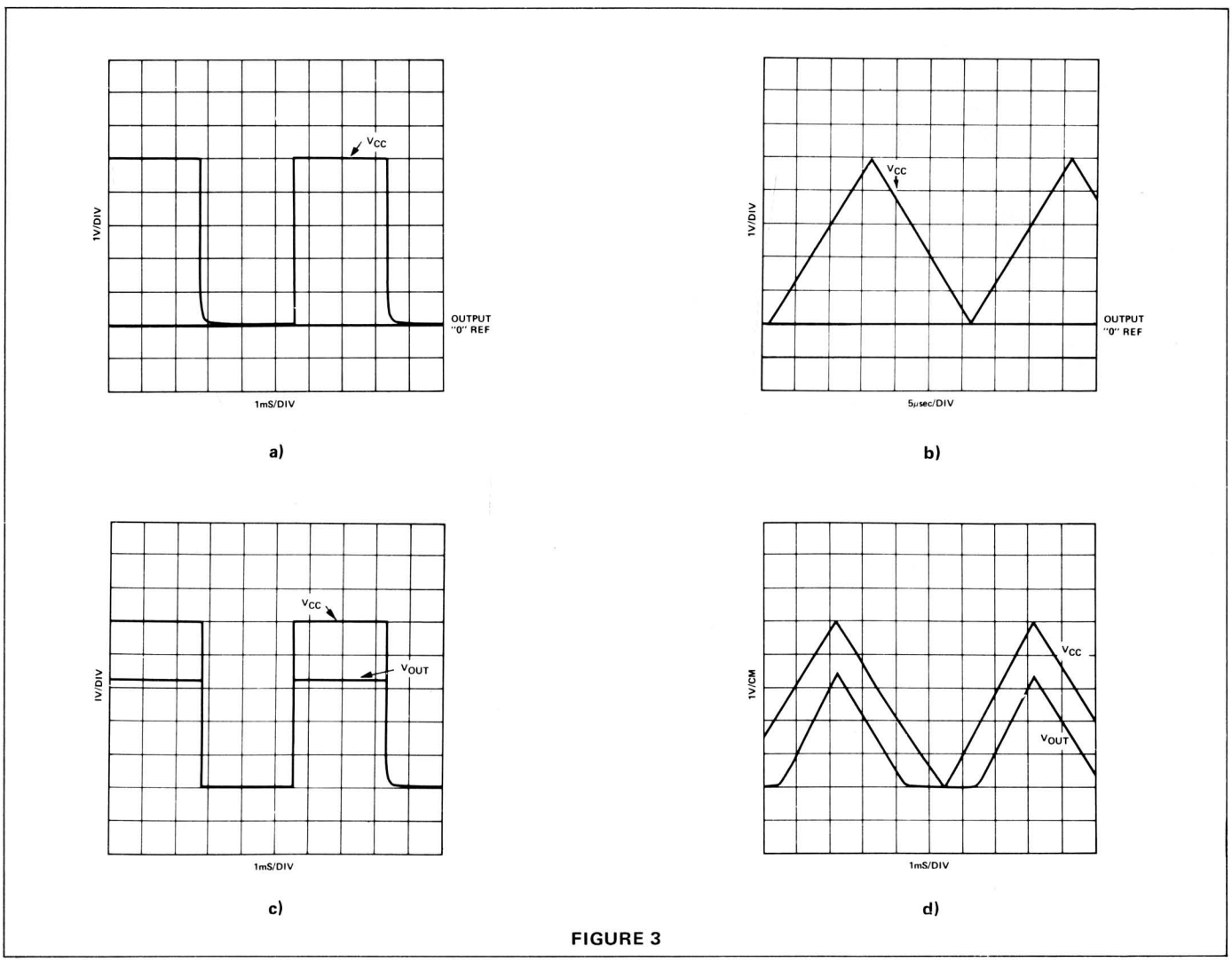


FIGURE 3

DESCRIPTION OF THE 8T24

The logic diagram of the 8T24 triple line receiver is shown in Figure 4. Each receiver may be strobed independently and has additional control logic to allow the output to be forced to a logical "0" by external control signals. Like the 8T23 line driver, the 8T24 line receiver is also TTL compatible and operates from a single 5V power supply.

Because the 8T24 is intended for use at the receiving end of digital transmission lines, the device has built in hysteresis to discriminate against line reflections and noise. The 8T24 has been designed with high input impedance and will contribute insignificant loading effects to the transmission line. This is an important factor when several receivers have to be driven by the same driver as in the party-line applications and bus-oriented systems.

8T24 TRIPLE LINE RECEIVER

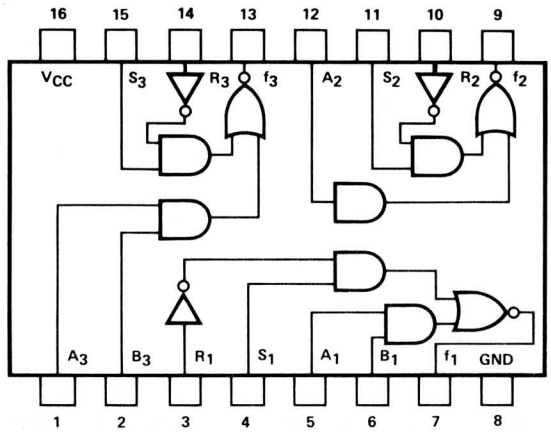


FIGURE 4

LINE RECEIVER REQUIREMENTS

Table 2 shows that the 8T24 meets the electrical characteristics as defined by the IBM interface specifications. As already mentioned under the 8T23 driver characteristics, at least 10 receivers can be driven by one line driver.

One area of the IBM specifications that should be clearly understood is that of threshold voltages. An input voltage of 1.7V or more shall be interpreted as a logical "1", and an input of 0.7V or less shall be interpreted as a logical "0". Therefore, having defined the minimum logical "1" level and the maximum logical "0" level the designer has to decide on the actual transfer curve most desirable.

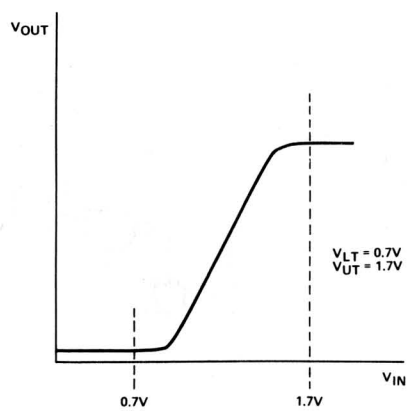
The 8T24 has been designed with hysteresis since it gives the highest noise immunity possible. Figure 5a shows a transfer curve for a hypothetical receiver without hysteresis whereas the 8T24 transfer curve is shown in Figure 5b. It can be seen that both approaches meet the same specification but that the 8T24 has greatly improved noise immunity as illustrated in Table 3.

LINE RECEIVER

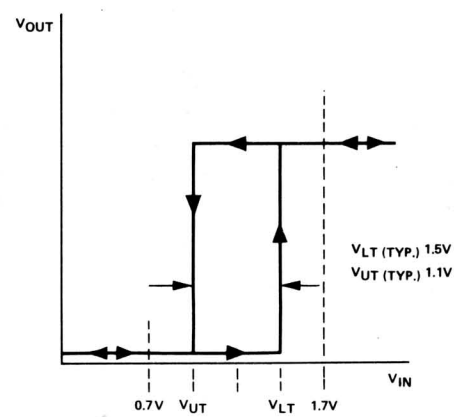
INTERFACE REQUIREMENT	IBM SPECIFICATION	8T23 SPECIFICATION	MEETS OR EXCEEDS IBM SPECIFICATION
$I_{IN}(1)$ LOGICAL 1 INPUT CURRENT AT 3.11V	0.42mA(MAX.)	0.17mA(MAX.)	YES
$-I_{IN}(0)$ LOGICAL 0 INPUT CURRENT AT 0.15V	−0.24mA(MAX.)	+5μA*	YES
$V_{IN}(1)$min MINIMUM LOGICAL 1 INPUT VOLTAGE	1.7V	1.7V	YES
$V_{IN}(0)$max MAXIMUM LOGICAL 0 INPUT VOLTAGE	0.7V	0.7V	YES
V_{IN}(max) MAXIMUM INPUT VOLTAGE — POWER-ON	7.0V	7.0V	YES
V_{IN}(max) MAXIMUM INPUT VOLTAGE — POWER-OFF	6.0V	6.0V	YES

* With 0.15V applied current direction is into the 8T14.

LINE RECEIVER TRANSFER CURVES



a) Transfer curve without hysteresis



b) Transfer curve with hysteresis

FIGURE 5

RECEIVER WITHOUT HYSTERESIS	SIGNETICS 8T24
$N_1 = V_1 - V_{UT}$, = 3.11V–1.7V, = 1.41V	$N_1 = V_1 - V_{UT}$, = 3.11V–1.1V, =2.01V
$N_0 = V_{LT} - V_0$, = 0.7V–0.15V, = 0.55V	$N_0 = V_{LT} - V_0$, = 1.5V–0.15V, = 1.35V

Where:

N_1 = Logical "1" DC Noise Margin
N_0 = Logical "0" DC Noise Margin
V_1 = Driver output voltage in the logical "1" state
V_0 = Driver output voltage in the logical "0" state
V_{LT} = Input threshold voltage when output is switched from a logical "0" to a logical "1"
V_{UT} = Input threshold voltage when output is switched from a logical "1" to a logical "0"

POWER–UP POWER–DOWN SEQUENCE FOR THE 8T24

The 8T24 line receiver has been designed to ensure that no spurious noise is generated during a normal power-up or power-down sequence. The receiver input will never require more than the specified input current and will not generate transients when turned on or off.

GENERAL SYSTEMS CONSIDERATIONS

A typical application of the 8T23 line driver and the 8T24 is shown in Figure 6. For an IBM interface the line has a characteristic impedance of 92Ω ±10% and is terminated at each end in its characteristic impedance by a terminating network. This may be a resistor presenting an impedance of 95Ω ±2.5% connected between the signal line and ground.

Fault-conditions on the transmission line will not damage 8T23 drivers or 8T24 receivers. When a signal line is accidently shorted the driver will current limit because of its built-in short circuit protection (ref. Figure 2). The receivers will not be damaged by over-voltages as shown in Table 2. In addition ground-shifts or noise up to -0.15V will not damage the receiver.

Party-line applications of multiple drivers and receivers are discussed in the 8T13 and 8T14 applications memo.

TYPICAL LINE–DRIVER LINE–RECEIVER APPLICATION

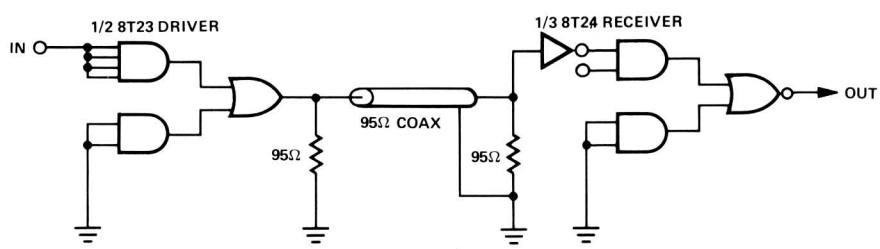


FIGURE 6

8T80, 8T90 AND 8T18 INTERFACE ELEMENTS

INTRODUCTION

TTL integrated circuits must, from time to time, communicate with external circuits and input-output hardware such as relays and lamps. Typically these devices may operate at higher voltage and/or power levels. Frequently, the need also exists to transmit digital data through areas with high noise levels. Thus, there is a need for interface circuits to communicate between logic and the external environment.

The 8T80 Quad 2-input interface gate and the 8T90 Hex-interface buffer can couple low level (typically 5V and 25mW) logic to a higher level (typically 28V and 280mW). Thus, the power level has been raised by over a factor of ten. The noise susceptibility has been reduced by a factor of ten and the signal is more closely matched to the medium power output requirements. The 8T80 and 8T90 couple low level logic information out of the protected logic area and provides the buffer isolation plus the advantage of power amplification. The information can now be transmitted through the high noise environment. If a signal needs to enter or re-enter a low logic area then the process needs to be reversed. The 8T18 performs the high to low level voltage translation. The 8T18 has an extremely stable (6.5V minimum) logic threshold and can entirely eliminate up to 6.5V of noise riding on top of the information signal. Thus, the 8T18 effectively couples the high signal down to the lower level while providing digital threshold noise separation and buffer isolation.

The 8T80 and 8T90 schematic and logic diagram are shown in Figure 1. These devices provide translation from TTL logic signals to high voltage output transistors. The input structure is a multiple emitter input transistor with only one input for the 8T90. The bare collector outputs permit a wide variety of loads to be used and, in addition, they facilitate paralleling of two or more devices to perform collector logic or driving higher current loads. The LV_{CO} voltage for the outputs is tested to be greater than 40 volts and this limit should not be exceeded even on a transient basis.

8T80 AND 8T90 SCHEMATIC AND LOGIC DIAGRAM

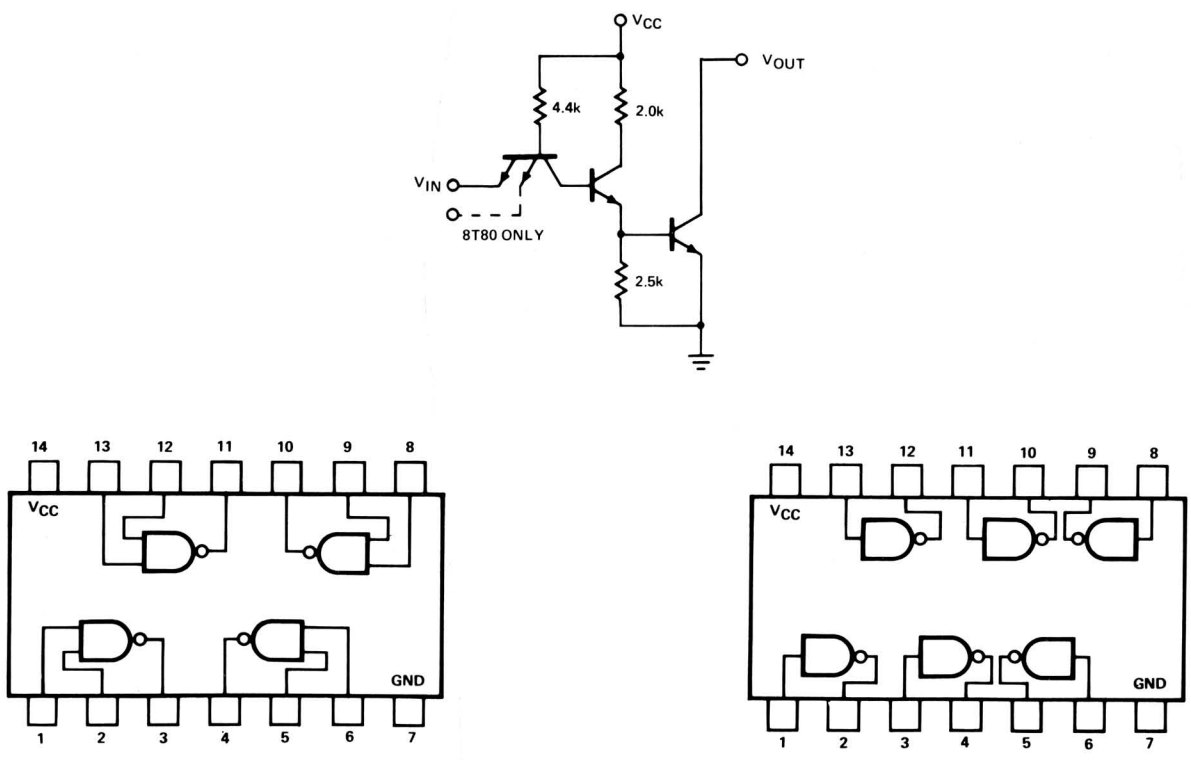


FIGURE 1

8T18 SCHEMATIC AND LOGIC DIAGRAM

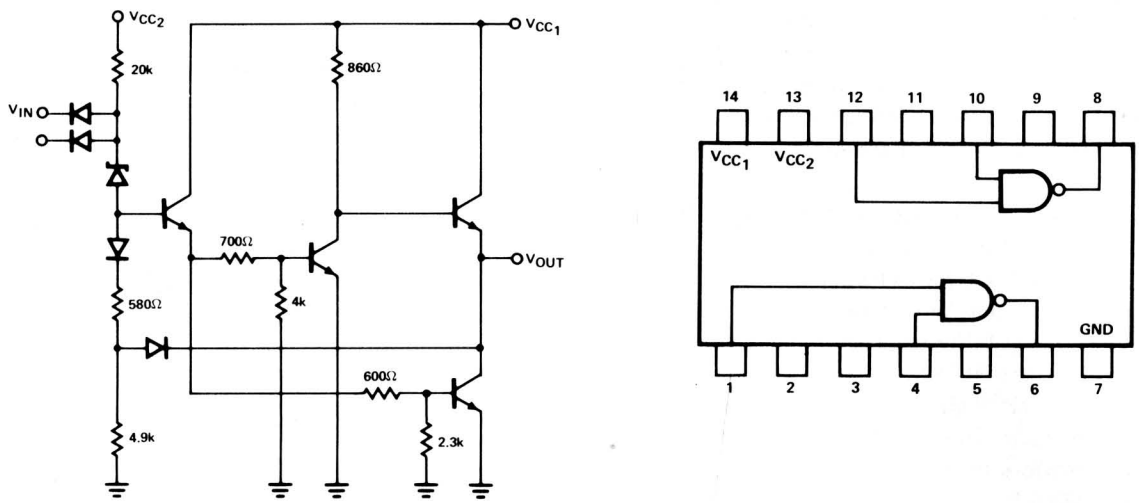


FIGURE 2

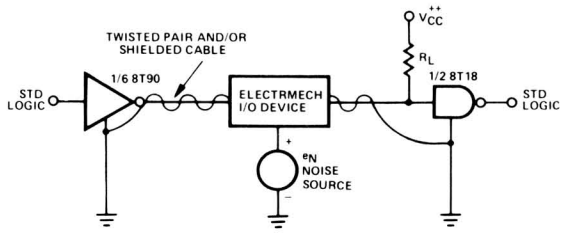
The 8T18 interface element complements the 8T90 in performing the opposite translation from high level to low level signals. Figure 2 shows the schematic and logic configuration. The terminal V_{CC_2} is returned to a power supply of 15V or more. If the V_{CC_2} voltage exceeds 30V a series current limiting resistor (limit current <2mA) or a shunt 20 to 30V Zener diode must be used. The input diodes are rated at 50V reverse breakdown. If input signals exceed or equal 50V, another diode must be added externally in series to protect the internal diodes from breakdown. An important fact about the 8T18 is that its threshold voltage (typically 7.4 to 7.8V) is independent of temperature. The various junctions being equal in number and opposite in polarity. Thus, the 8T18 is an accurate high level threshold detector.

APPLICATIONS
HIGH LEVEL BUFFER INTERFACE

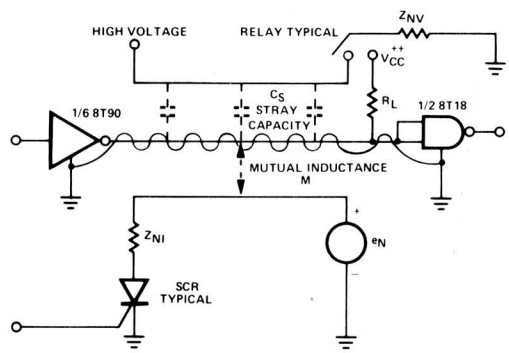
The most general application for the 8T80/90 and 8T18 interface is as buffer elements to provide isolation between low level integrated circuit logic and the high level noisy outside world. The most common causes of output to input noise are shown in Figure 3. In Figure 3a, logic is being transmitted to a typical electromechanical device such as a typewriter, tape punch, printer, tape reader, etc. The electromechanical device frequently will have high energy solenoids, SCR, etc., that tend to generate a noise voltage between the logic ground and the device ground. Logic output lines are well isolated from the internal logic because the 8T90 and 8T18 are used.

Note that the 8T90 collector pull-up resistor is connected at the receiving end (i.e., near the 8T18). This helps to lower the 8T18 input impedance. Since there is no connection back into the logic area (even the power supply is isolated) the collector noise is not coupled into the low level logic. The most critical interface is the connection from the electromechanical device or transmitting end into the low level logic area. Here the noise source is in series with signal and looks directly into the logic input circuitry. Without the 8T18 high threshold buffer element, the noise would only have to overcome the normal 1 to 2V threshold to cause false inputs. However, the 8T18 has an input threshold guaranteed to be at least 6.5V worst case and conducted noise spikes up to 6.5V will not cause false inputs.

COMMON SOURCES OF NOISE



a)



b)

FIGURE 3

Figure 3b depicts an application where one logic area is connected to another logic area. The distance between the two areas may be as much as one hundred feet or more and may pass through areas of high electric and magnetic fields. The magnetic and electric fields plus conduction are responsible for almost all noise coupling, but seldom is electromagnetic radiation the source of noise coupling. The electric field couples via stray capacitance and Figure 4 shows the stray capacitance coupling noise from a voltage source e_n. The noise source could be a voltage being switched by relays, or any potential varying rapidly in time with respect to ground which will couple some voltage into the signal line via the stray capacity.

ELECTRIC FIELD COUPLING

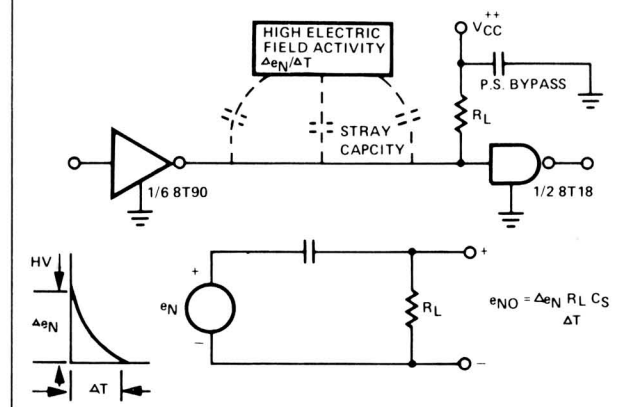


FIGURE 4

The stray capacity can be minimized by separating signal line physically apart from potential varying circuits and by shielding. Some stray capacitance will remain, however, and the voltage coupled can be approximated by

$$e_{no} = \frac{\triangle e_n R_L C_S}{\triangle T}$$

Where Δe_n is the change in potential, R_L is the logic load resistor (8T90 collector pull-up resistor), C_S is the residual stray capacity, and Δ T is the time it takes the voltage to change.

The noise is coupled during the logic "1" level. During the logic "0" level, R_L is shunted by the 8T90 collector saturation resistance.

Considering the example in Figure 5, the logic signal line is run in the proximity of a high voltage line that is switching 10mA by a relay. A switch speed limiting network consisting of a 150 ohm resistor and a .0067μFcapacitor has been added to slow the switching speed and has a time constant of 1μs.

Given the following information:

e_n = 150V
T = 150 X 0.0067 X 10^{-6} = 1μs
e_{no} = 6.5V max. permissible
R_L = 1.9K min. at 28V

EXAMPLE ELECTRIC FIELD COUPLING

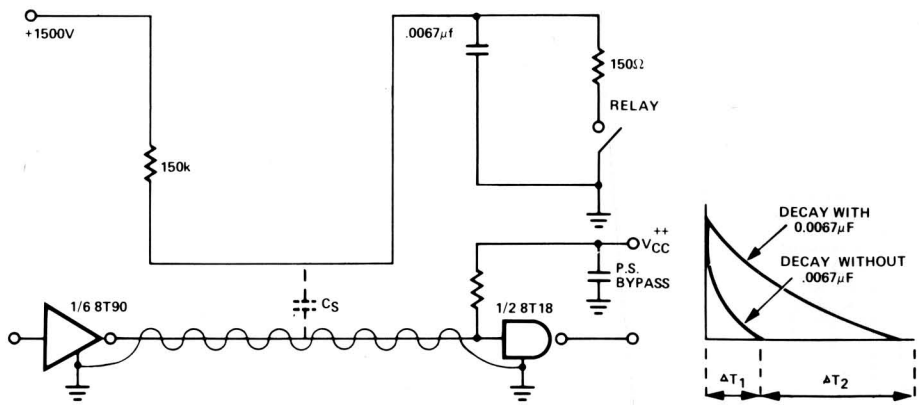


FIGURE 5

The maximum permissible stray capacitance is:

$$C_S = \frac{6.5 \times 10^{-6}}{1.5 \times 10^2 \times 1.9 \times 10^3} = 23pF$$

Good layout techniques will easily hold the stray capacitance below this value.

The above example illustrates the mechanism of electric field interference coupled into signal lines and the techniques used to minimize the coupling. In summary, the following action will minimize electric field coupling:

1. Minimize stray capacitance C_S
   (a) Avoid bringing signal lines close to conductors with varying potentials.
   (b) Use as much shielding as is economically feasible.
2. Slow rate of electrostatic field collapse, ΔT, by use of networks as shown in the example.
3. Hold the resistive impedance, R_L, as low as practically feasible.
4. Use the high threshold gate, 8T18, to provide the highest possible voltage margin.

To understand the mechanism of inductive noise coupling into the logic lines consider the circuit in Figure 6a. All circuits must have self inductance just as all circuits must have capacitance. There exists then some mutual inductance between the signal circuit and the current noise source I_n. Mutual inductance is defined as:

$$M = k\sqrt{L_S L_N},$$

MAGNETIC FIELD COUPLING

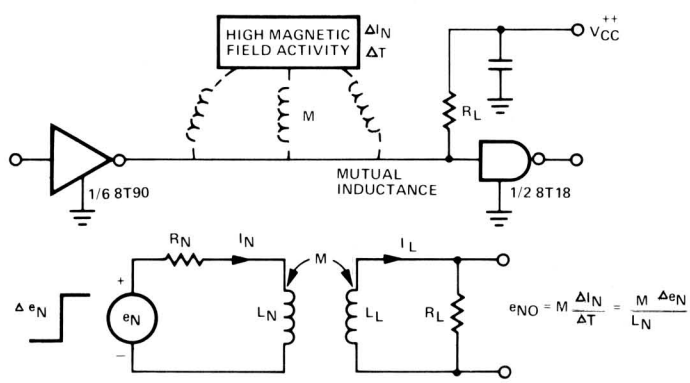


FIGURE 6

Where k is the coefficient of coupling and L_S and L_N are the signal and noise circuit self inductances. The best defense against noise is to keep the mutual coupling low. The coefficient of coupling is reduced by using twisted pair wires and magnetic shielding of both the noise circuit and the signal circuit. The self inductances are minimized by using twisted pairs and the largest wire size economically feasible. A simplified equivalent circuit is shown in Figure 6b. Note that the induced voltage due to inductive coupling appears only during the "0" level. During the "1" level, R_L is in series with the off resistance of the 8T90. The analysis assumes that the mutual inductance is very much smaller than the self inductances. The result indicates that the induced voltage is directly proportional to the current switched, the mutual coupling and inversely proportional to the time taken to switch. Written in another form the equation indicates that the induced voltage is proportional to the mutual inductance divided by the noise circuit's self inductance times the voltage being switched. Note that the induced voltage is not a function of R_L, the signal lead resistive impedance. From these equations, one can summarize the following:

1. Keep signal lines physically separated (reduce coefficient of coupling or mutual inductance).

2. Minimize the signal inductances by using largest practicable wire size and using twisted pair or coax where necessary.

3. Slow down the current switching rate T (e.g., insert charging reactors thereby increasing L_N).

4. Use the high threshold logic element 8T18 to increase noise margin.

TYPICAL OUTPUT VOLTAGE VS. OUTPUT CURRENT

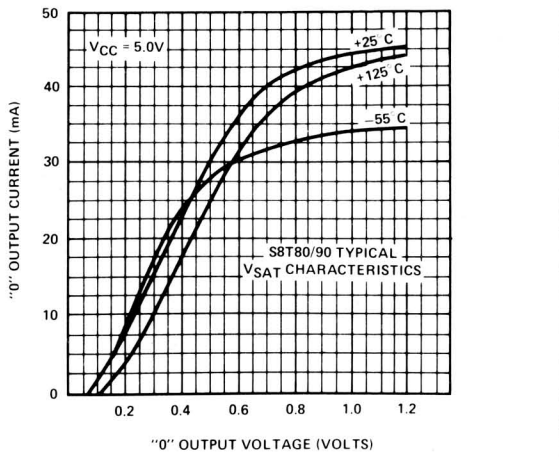


FIGURE 7

ALL PURPOSE DRIVER

The 8T90 is the most versatile integrated circuit device for output interface applications in the 8000 family. To utilize the element to its utmost capability, some understanding of the limitations of output voltage and current are necessary. A curve of typical output current versus saturation voltage and temperature is shown in Figure 7. The driver current rating at a specific operating point is given in the data sheet. However, if other operating points are desired, then the curve of Figure 12 indicates output currents expected versus saturation voltages. In designing for maximum current rating the maximum device dissipation rating of 310 milliwatts at 125°C must not be exceeded for the dual-in-line silicone A package.

This figure was arrived at by substituting design data into the relationship:

$$T_{j\ max} = T_A + P_{max} \times \Theta_{J\text{-}A}$$

Where:

T_j max = max. allowable junction temperature (175°C for A package)

T_A = ambient temperature

P_{max} = maximum allowable power dissipation

$\Theta_{J\text{-}A}$ = junction to ambient thermal impedance (0.16°C/mW for A package)

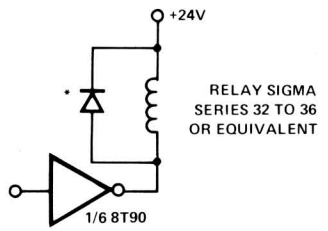
Since each gate draws 20mA from the V_{CC} power supply when turned on with zero collector current, the total available collector power dissipation can be calculated. If all six inverters are on at the same time, the IC is dissipating (6 X 20) = 120mW and 310mW – 120mW or 190mW are available for collector circuit dissipation at 125°C before thermal considerations become important.

RELAY DRIVER

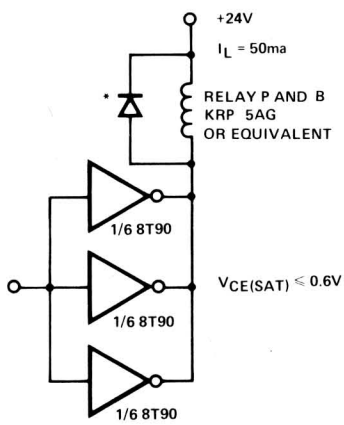
Figure 8 shows the 8T90 used in a relay driver application. The free wheeling diode is used to dissipate the energy stored in the relay inductance. When the relay is released the 8T90 collector current is diverted through the IN3064 diode, thereby restricting the induced voltage. Due to the three transistor TTL structure of the 8T90 (Figure 1), the reverse transfer is negligible and noise existing on relay wiring, etc., will not be coupled back into the logic. Thus, the inverter performs the function of interfacing and provides buffer isolation.

In Figure 8a, a low power relay is driven by a single inverter stage. In Figure 8b, three drivers are paralleled to drive a 10 ampere double throw general purpose relay. The expected saturation voltage is less than 0.6V and the total dissipation in the three circuits is 3 X 20 + 30 = 90 milliwatts, below the total power dissipation capability.

8T90 RELAY DRIVER APPLICATION



a)



b)

* Diode IN 3064

FIGURE 8

LAMP DRIVER

Another application of the 8T90 Hex Inverter is as an incandescent lamp driver shown in Figure 9. For lamps requiring less than 20mA drive, one driver is sufficient but if more current is required, drivers may be paralleled. Since the output transistors are beta-limited as illustrated in Figure 7, the inrush-current restrictions are not severe because a natural current-limiting effect will take place in the output transistors.

8T90 LAMP DRIVER APPLICATION

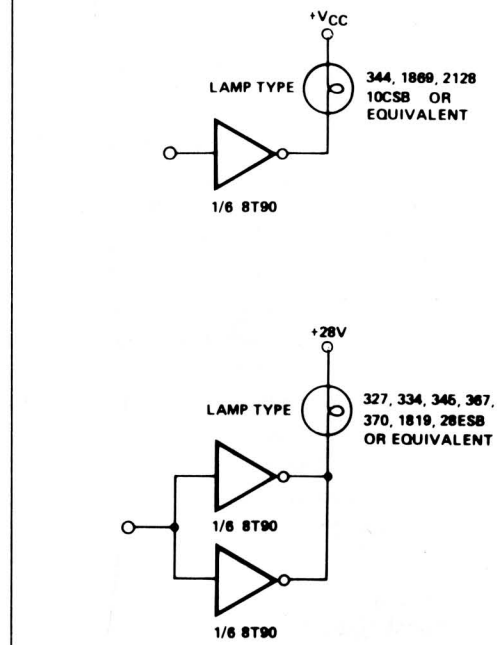


FIGURE 9

MILLER INTEGRATOR

The 8T90 may be used as a Miller integrator. The basic circuit is shown in Figure 10. The down ramp is independent of the load resistor R_L. This circuit is valuable for use as an integrator for lamp circuits and in general slowing down the output driver. The ramp can be approximated as shown in Figure 10.

BASIC INTEGRATOR CIRCUIT

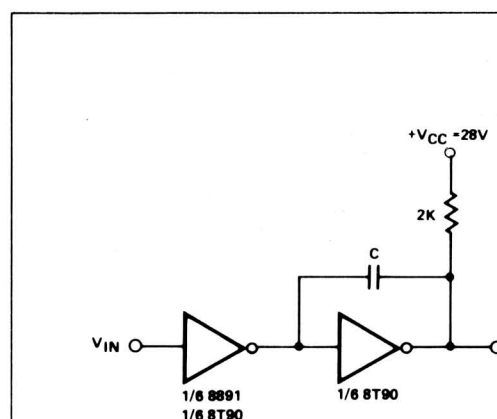


FIGURE 10

BASIC INTEGRATOR CIRCUIT (Cont'd)

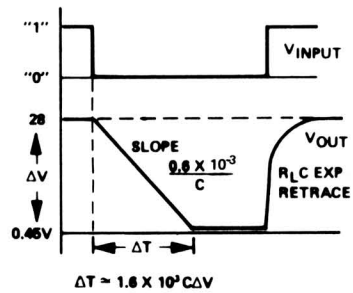


FIGURE 10 (Cont'd)

8T80 QUAD GATE INTERFACE ELEMENT

The 8T80 is a quad 2-input NAND gate whose output structure and drive capability is identical to that of the 8T90. Since there are two less stages per package the 8T80 can dissipate proportionately more power per stage relative to the 8T90. Figure 11 shows some latching-driver applications of the 8T80.

8T80 QUAD GATE APPLICATIONS

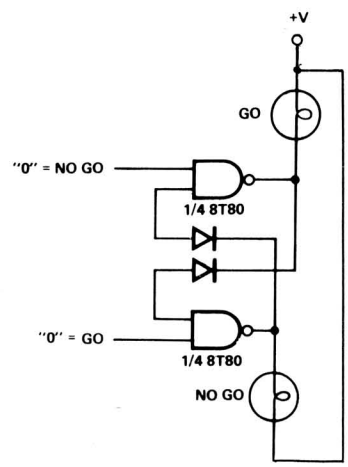
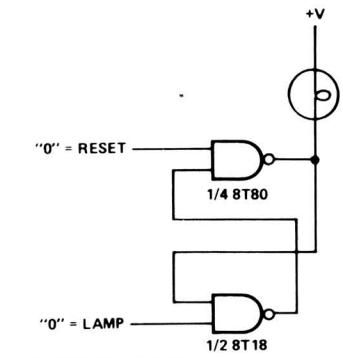


FIGURE 11

8T80 QUAD GATE APPLICATIONS (Cont'd)



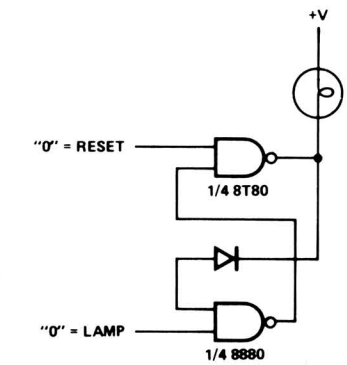
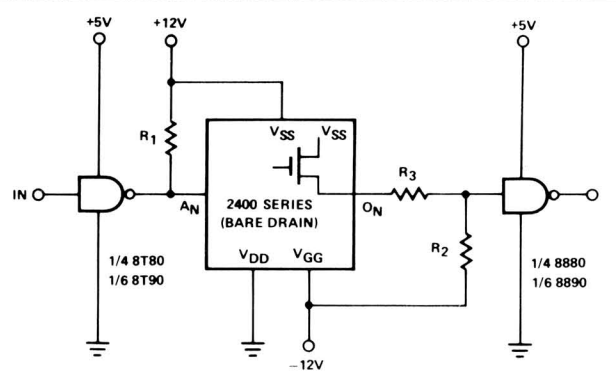


FIGURE 11 (Cont'd)

TTL–MOS–TTL INTERFACE

To interface with metal gate MOS circuits the 8T80 and 8T90 are very useful since output swings of 12V can be easily accommodated. To translate from the MOS output to TTL only a standard 8880 gate is needed. An application is shown in Figure 12.

TTL–MOS–TTL INTERFACE



NOTES:
1. R_1 may range from 680Ω to 33K, typically 3.3K is satisfactory.
2. R_2 6.8K for a standard TTL (I_0 IN = 1.6mA)
3. R_3 = 2.2K

FIGURE 12

POSITIVE TO NEGATIVE VOLTAGE TRANSLATOR

The 8T18 high-to-low voltage interface elements work perfectly in this application if the following connections are made: ground to a -5V ± 5% supply, V_{CC1} to ground and V_{CC2} to a +15V ± 5% supply for -55°C to +125°C operation or V_{CC2} to a +10V ± 5% supply for -25°C to +125°C operation. See Figure 13a. Thus, the designer has the capability of going from +5V supply digital systems such as TTL or DTL to -5V supply systems. An external PNP can be added to the output permitting large voltage swings (Figure 13b).

POSITIVE TO NEGATIVE VOLTAGE TRANSLATOR

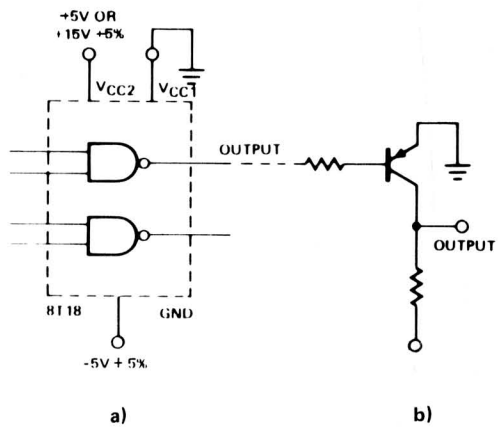


FIGURE 13

The 8T80 and 8T90 can be used to translate from negative to positive voltage logic systems as shown in Figure 14. The inputs to the 8800 gates have diffused input clamping diodes to limit negative input excursions.

NEGATIVE TO POSITIVE VOLTAGE TRANSLATOR

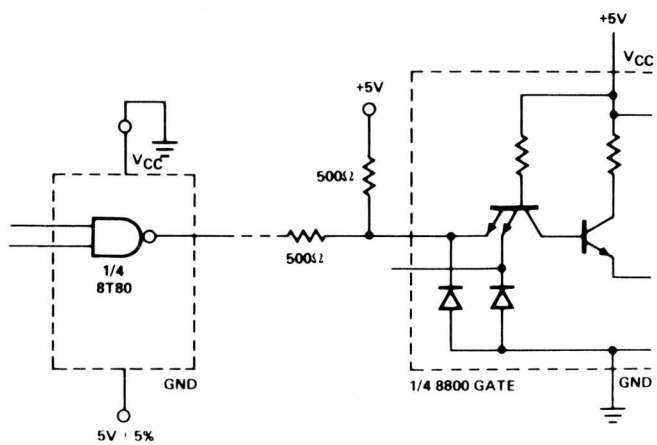


FIGURE 14

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