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LB-974

TRANSISTORIZED SYNC SEPARATOR CIRCUITS FOR TELEVISION RECEIVERS

RADIO CORPORATION OF AMERICA
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Transistorized Sync Separator Circuits for Television Receivers

Approved

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Introduction

This bulletin presents transistorized sync separator circuits which appear to meet commercial requirements for operation under both good and adverse conditions. Tests on a limited number of transistors indicate good interchangeability and satisfactory performance up to 60 degrees C. The impulse noise immunity of sync separators is discussed. A method of using diode switching to control the time constant of a single-transistor separator for optimum impulse-noise performance is given.

Transistor collector voltage ratings must be at least equal to the level of sync output voltages required. High-frequency response on the order of that of the RCA experimental SX-160 is needed in the horizontal separator for good sync rise-time. Low I_{eo} and I_{co} are desirable, but most of the circuits described will tolerate high temperature leakages on the order of 50 to 100 microamperes.

Because of the abrupt low-voltage "knee" of the junction transistor, one transistor will produce double-clipped sync. Since this function is usually accomplished with a two-stage vacuum tube amplifier, the use of a transistor results in increased circuit simplicity.

General Discussion

Few circuits in a television receiver have shown as much variety as those for sync separation and a.g.c. This has resulted from the efforts of many engineers to devise economical circuits which will perform reliably under a wide variety of conditions. Some of these conditions encountered in the field are listed below:

1. A signal strength range on the order of 100,000 to 1.
2. Variations in sync percentage from the nominal 25 per cent.
3. Variation in tube (or transistor) characteristics including initial characteristics, aging, changes with temperature.
4. Variation in gain of associated circuits such as the r-f, i-f, and video stages.
5. Variations in line voltage.
6. Impulse noise of various types.
7. Airplane flutter.
8. Reflections and multipath reception.
9. Various degrees of picture contrast desired by user.

Vacuum tube circuits have been developed which meet these conditions in a reasonably satisfactory manner. Although such circuits may be relatively uncomplicated in structure, they are the result of much engineering and field testing, and make optimum use of the characteristics of the particular tubes employed.

Transistors differ from vacuum tubes in many important respects. As a result, most of the vacuum tube circuits will not work ef-

fectively with transistors. The purpose of this study has been to investigate the characteristics of transistors which are relevant to sync applications and to develop circuits which will utilize these characteristics to provide optimum performance at reasonable cost. Certain transistor characteristics such as low input impedance, uncontrollable forward collector conductivity, temperature sensitive leakage, and limited voltage ratings generally represent disadvantages for sync applications. On the other hand, the high transconductance, sharp cutoff and saturation characteristics, and the absence of heaters, represent definite advantages for transistors. Also, the existence of both p-n-p and n-p-n transistor types offers increased flexibility in devising circuits. Thus the application of transistors to sync circuits presents both new problems and new opportunities to the circuit designer.

The Junction Transistor as a Pulse Amplifier

All of the three basic transistor amplifier types--common emitter, common base, and common collector--can be used as sync amplifiers. The common emitter connection gives the poorest rise and fall times for a given transistor. However, since it is the only one giving both voltage and current gain, both of which are usually required, it is the most useful. Most of the following discussion of pulse amplifier characteristics is therefore devoted to the common emitter type.

Fig. 1a illustrates the common emitter circuit and Fig. 1b shows one form of its equivalent circuit.[1] Since the vertical straightness of the received picture depends on the timing accuracy of the sync pulses, reasonably good rise-time of the horizontal sync amplifier is highly desirable. An important limitation on rise-time is set by the time constant of $r_{bb'}$ and $c_{b'e}$. A low-frequency transistor such as the 2N34 may have a rise-time actually in excess of the 5 μsec width of horizontal sync when operated with common emitter.

[1] *LB-915, A P-N-P Triode Alloy Junction Transistor for Radio-Frequency Amplification.*

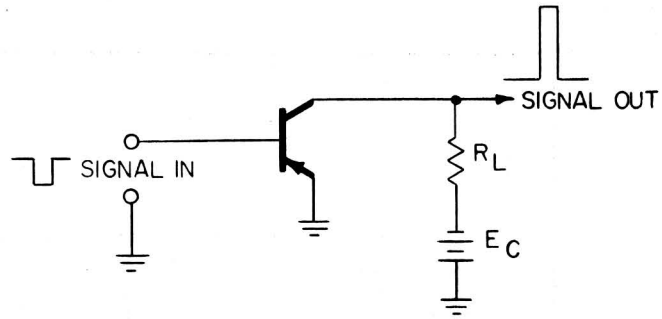

Fig. 1a - Common-emitter circuit.

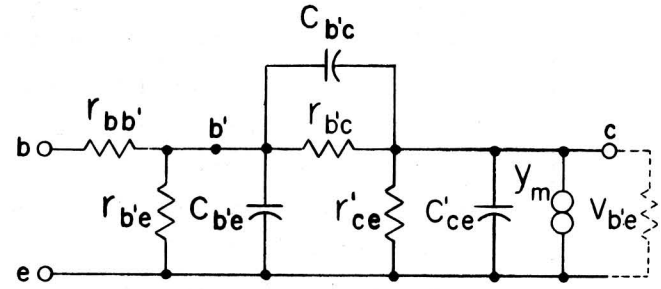

Fig. 1b - Pi-equivalent circuit.

TYPICAL VALUES FOR I_C = 1 MA

		2N34	SX-160
$r_{bb'}$	Ohms	250	75
$r_{b'e}$	Ohms	1000	500
$c_{b'e}$	μμf	10,000	1000
$r_{b'c}$	Meg	1	0.1
$c_{b'c}$	μμf	35	10
g_m	Mhos	.032	.032

Fig. 1 - Common-emitter circuit and pi-equivalent circuit.

The 10 to 90 per cent rise and decay-times of the medium-frequency experimental SX-160 with a 10,000 ohm collector load are on the order of 2 microseconds. Both rise and decay-times increase with increasing collector load resistance as indicated in Fig. 2. The rise-time can be reduced greatly by overdriving, as will be discussed later. The equivalent circuit of Fig. 1b indicates that any driving source resistance will lengthen the rise-time by effectively adding to $r_{bb'}$. Tests on an SX-160 substantiated this as shown in Fig. 3.

Fig. 4 illustrates the collector family of curves for a junction transistor. A fortunate

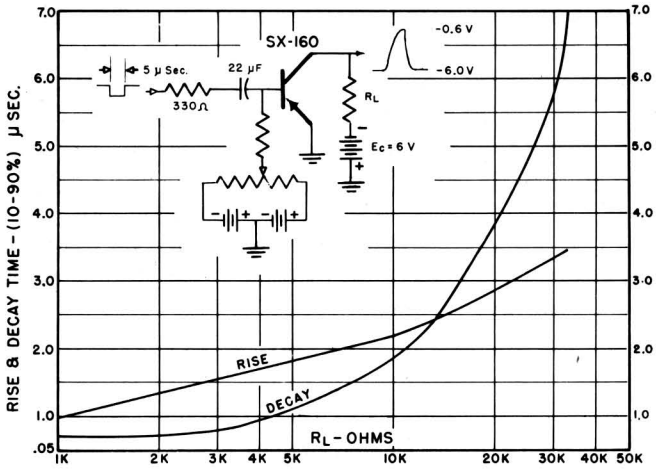

Fig. 2 - Rise and decay time vs collector load.

aspect of this characteristic for sync separators is the abrupt knee which occurs near zero collector voltage. Thus an amplifier with the proper load may be driven into increasing collector conduction until abruptly limited by collector voltage saturation. Such an amplifier, when driven from cutoff to saturation, produces a double-clipped output with an amplitude only a few tenths of a volt less than the collector supply voltage. The relatively flat collector characteristic above the knee is a result of the fact that the current carriers passing through the base layer to the collector travel by diffusion instead of being attracted by an electrostatic field as is the case in a vacuum tube. The value of the collector voltage thus has little effect on the collector current as long as it is sufficient to attract the carriers that have reached the collector junction.

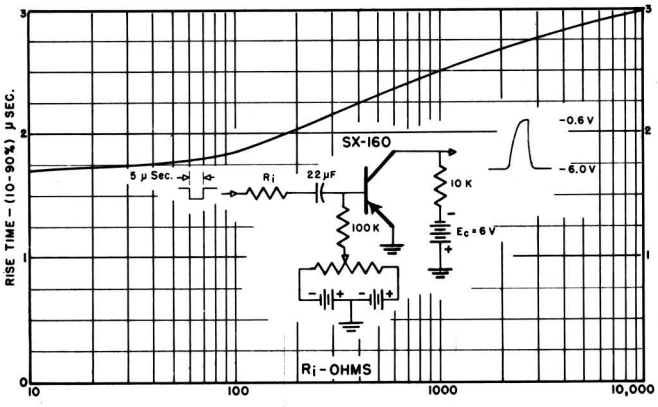

Fig. 3 - Rise time vs external base resistance.

Pulse-driving a transistor into collector saturation modifies both the rise and fall-time at the output. The application of a pulse which drives the base-emitter junction further in a forward direction than is necessary just to saturate the collector will be called *overdriving* the transistor. Overdriving produces a marked decrease in rise-time. As an example, applying an input signal voltage double that required just to saturate the collector of an SX-160 reduced the rise-time from 2 μsec to 0.2 μsec. Lesser amounts of overdriving will produce lesser degrees of pulse steepening. The variation in rise-time as a function of base-driving current in excess of that required to saturate the collector on sync tips is given

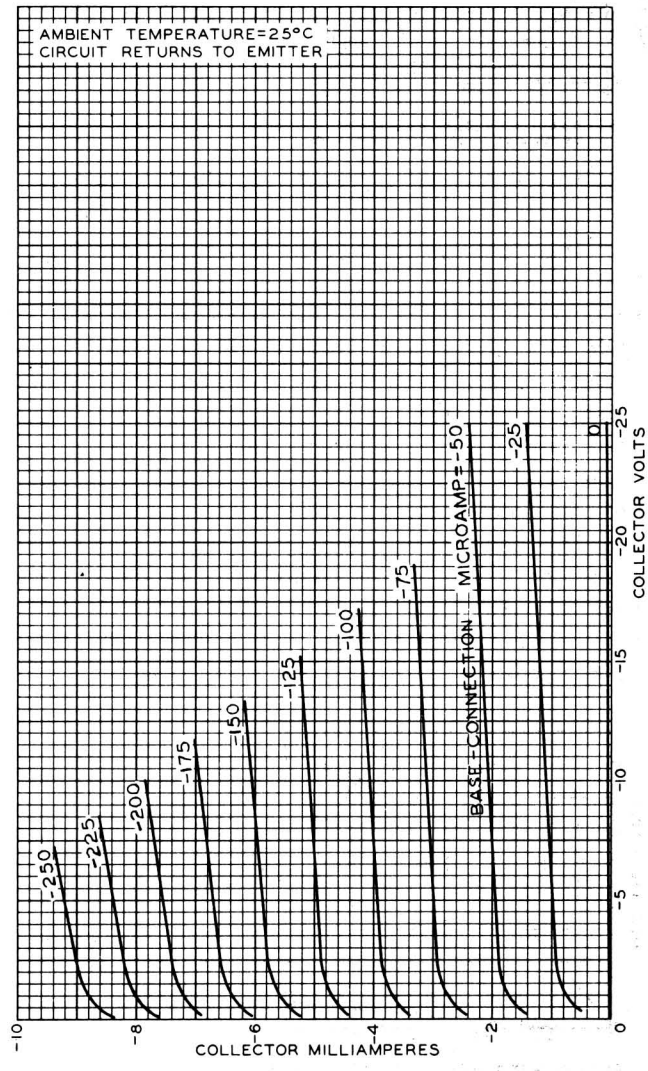

Fig. 4 - Typical junction-type transistor characteristics.

in Fig. 5 for an SX-160 and a 2N34. Since the output transistor of a sync separator will normally be overdriven to some extent to achieve double clipping, a considerable degree of pulse steepening will result. However, the use of an inherently low frequency transistor which requires a large degree of overdriving to produce an acceptable rise-time is wasteful of gain and has a deleterious effect on the trailing edge of the output.

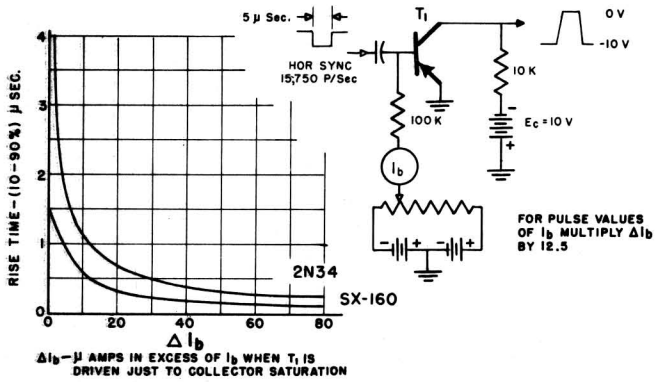

Fig. 5 - Rise time with overdriving.

The further effect of overdriving a junction transistor is that the trailing edge of the output pulse may be delayed, i.e., the pulse may be effectively widened. This effect has been called "back-porch" effect. Back-porch results from the fact that, while collector saturation limits the collector current to a value equal to the supply voltage divided by the load resistance, overdriving produces a minority carrier current flow into the base in excess of this limit. Some of the excess carriers are thus stored in the base and continue to flow to the collector after the input signal has returned to zero or reversed. Serious back-porch effect shifts the average timing of the sync output pulses and will cause a phase shift in many types of horizontal phase detectors. Other types of phase detector work primarily from the front portion of the sync pulses and will be little affected. In any case it is possible with a medium-frequency transistor such as the SX-160 to get adequate overdriving for good limiting and rise time without producing serious back-porch effect.

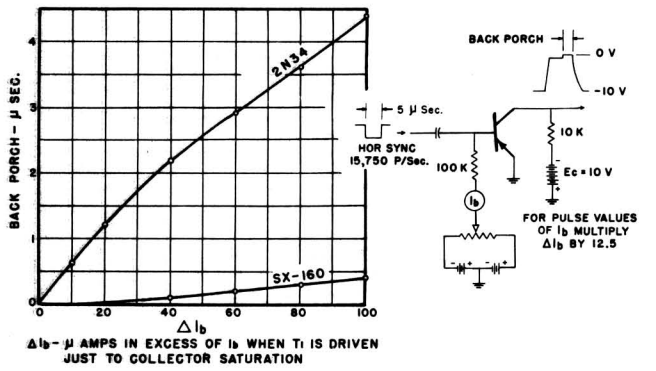

Fig. 6 - Back-porch width with overdriving.

Driving Source

Transistors operated with common emitter or base have a low input resistance. The particular value of resistance varies considerably depending on transistor characteristics, circuit parameters, and operating current. An average SX-160 as typically operated in a sync separator with common emitter and an 8200-ohm collector load has an input resistance on the order of 500 to 1000 ohms within its amplifying range. Beyond the saturation point the input resistance falls to a fraction of this value; below cutoff it may rise to over a megohm. It is evident that a low-impedance video source is desirable to drive transistorized sync and a-g-c circuits most effectively. Since at low power levels a transistor is essentially a current-driven device, a high source impedance with a signal voltage proportionally increased to supply the required signal current might also be satisfactory. However, there are two limitations to the use of such a high-impedance source: (1) the high video amplitude existing between sync pulses while the transistor is at cutoff will cause increased base-to-emitter leakage, thus disturbing the bias, and (2) the source impedance adds to the base resistance to produce, in conjunction with $C_{b'e}$, a longer rise-time of the output sync pulses.

It seems basic to a-g-c circuits that the video signal must be d-c coupled to the a-g-c rectifier or amplifier. Otherwise a sudden increase in signal strength can overload the i-f amplifier, reduce the a-c video component, and block the receiver as a result of the faulty information derived from the a-c signal. Since transistors will not withstand the normal plate voltages encountered in a television

receiver, this means that the video signal applied to an a-g-c or combined sync and a-g-c transistor circuit must come from a source close to ground potential.

One obvious source of such a video signal is the second detector load. Since the transistors tested had a base-to-emitter capacity on the order of 15 μμf in the cutoff condition, such a transistor must be tapped down at least to the mid-point of the detector load to prevent undue capacitive loading. Unfortunately, the detector signal level in terms of video current available to the separator is not sufficient to operate the more economical separator circuits. A further disadvantage of this signal source is that any impulse noise present has not yet been clipped by the first video amplifier.

A second possible video source is from a resistive divider from video plate to ground as shown at point A of Fig. 7a. For some separator and a-g-c circuits this source is quite satisfactory. However, since the impedance of the divider must be high compared with the plate-to-B+ load to maintain the necessary video plate voltage, only a fraction of the total video plate current is available to the transistor circuits. In cases where the signal source need not be near d-c ground, as in a capacity-coupled separator, the full video signal current is available from a tap (B) on the normal video plate load.

A third video source which eliminates most of the disadvantages listed above is shown in Fig. 7b. The voltage developed across R_1, the normal cathode resistor, is not usually sufficient to supply the sync and a-g-c circuits. An additional resistor, R_4, is added to increase the video voltage at the cathode. This does not introduce degeneration since it is not in series with the grid-to-cathode voltage applied from the second detector load. Taking the signal from point C, the source impedance is low and grounded and carries the full video current in V_1. Optionally, a variable resistance R_5 can be inserted as a contrast control. As the resistance of R_5 is increased, the voltage across it increases, but the voltage across R_4 decreases as degeneration decreases the gain of V_1. The result is that the voltage to the separator can be kept relatively constant. If the resistance of R_5 is made too great, the current available to the separator may be insufficient, but a fair range of contrast control may be achieved. In this circuit the capacity of the V_1 grid lead to ground is effectively increased by the added video voltage developed across the R_4. This capacity should therefore be kept as low as possible.

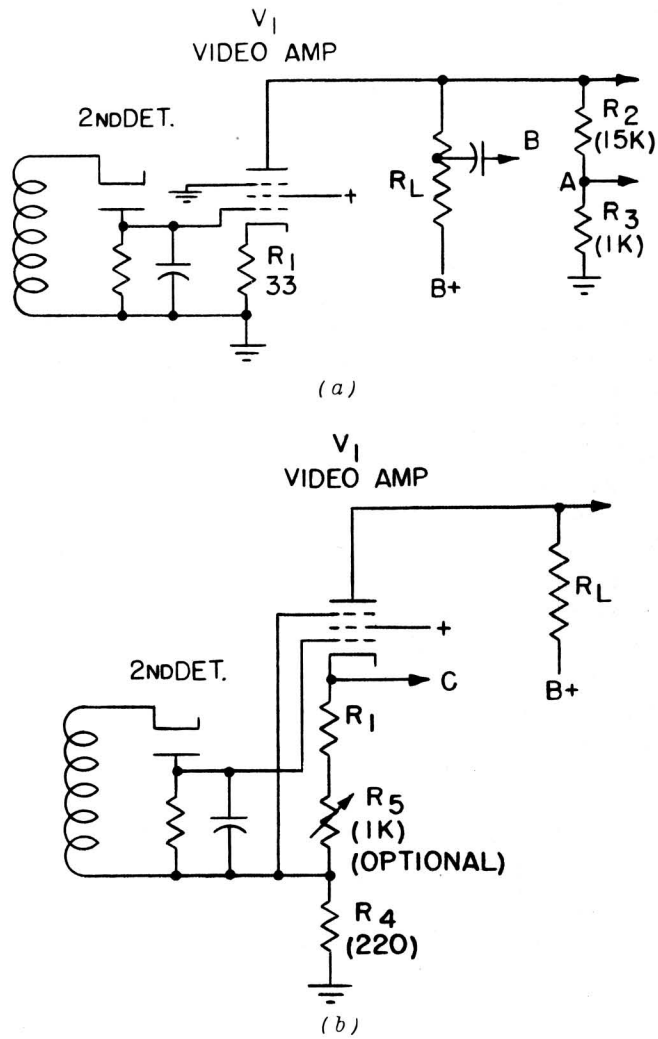

Fig. 7 - Driving signal sources.

Two-Stage Sync Separators

A critical factor in a transistorized sync separator is maintaining the proper separation bias level. Even with a good a-g-c system the video level applied to the separator will change considerably with changes in line voltage, a-g-c control setting, and the extreme range in signal levels which may be encountered. Fig. 8 illustrates how the separation level,

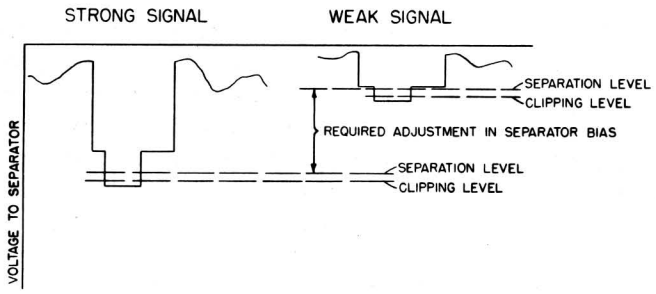

Fig. 8 - Adjustment of separation level.

i.e., the level where the separator begins to conduct, must change with signal level. This obviously requires the use of self-adjusting rather than fixed bias.

Fig. 9 illustrates one form of two-stage sync separator. The emitter current flowing through R_1 establishes an emitter bias which biases the base-emitter junction of T_1 in the reverse direction except during sync. Collector current flows during sync to produce sync output pulses across R_2. E_2 and R_2 are proportioned to avoid collector saturation, so that the pulse amplitude across R_2 varies somewhat with variations in input amplitude. The emitter current likewise varies with signal amplitude so that the bias is kept at the proper level for separation on all signals. This circuit is analogous to the cathode-biased vacuum-tube separator frequently used.

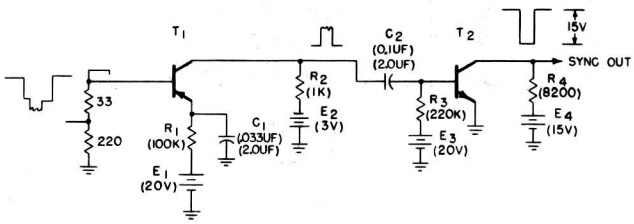

Fig. 9 - Two-stage sync separator.

The first separator in Fig. 9 is relatively non-critical of transistor characteristics, assuming that the transistor has adequate high-frequency response to give the required rise time. The collector current vs base-to-emitter voltage characteristic at low currents has been found fairly constant from unit to unit, at least for a given transistor type. The input resistance varies considerably, particularly with variations in α, but this does not affect the circuit operation if the signal has a sufficiently low impedance. An advantage of placing bias resistor R_1 in the emitter circuit is that if the d-c impedance of the base circuit is low, the collector-to-base leakage current, I_{co}, does not appreciably affect the bias. Between sync pulses the base-emitter junction is biased in the reverse direction, and any leakage at this junction, I_{eo}, will flow through R_1. In a transistor whose characteristics are satisfactory for the circuit, I_{eo} should be small compared with the average emitter current, and hence have only a minor effect on bias.

In the circuit of Fig. 9 a second transistor T_2 is used to amplify and limit the amplitude of the pulses across R_2. T_2 is operated so that it is driven to saturation during sync by any usable signal. This provides sync of uniform amplitude and cuts off any noise pulses at sync level. Since the sync has been completely separated from the blanking pulses by T_1, it would be possible to operate T_2 with fixed bias or with direct coupling. However, the bias would have to be set so that T_2 would saturate on the sync of weak signals; this means that on a strong signal T_2 would be heavily overdriven. The result is a considerable widening of horizontal sync on strong signals due to back-porch effect. Such heavy overdriving is avoided by using self-bias on T_2, as is shown in Fig. 9. Bias E_3 is adjusted so that T_2 will saturate on very weak sync. A transistor driven to collector saturation ceases to give normal transistor action since the collector current is fixed. The base-to-emitter characteristic under this condition is like that of a junction diode and has a low forward resistance. The effect of saturation on input resistance is shown in Fig. 10. The input circuit of T_2 thus functions as a clamp circuit, producing sufficient reverse bias so that T_2 is always overdriven but never to the extent of producing excessive back-porch widening of the sync output. The average base current I_b due to conduction during sync, charges C_2 and must equal the currents discharging C_2:

$$I_b = I_3 + I_{co} + I_{eo}$$

where I_3 = current through bias resistor R_3

I_{co} = collector junction reverse leakage current

I_{eo} = emitter junction reverse leakage current

The base current actually flowing during

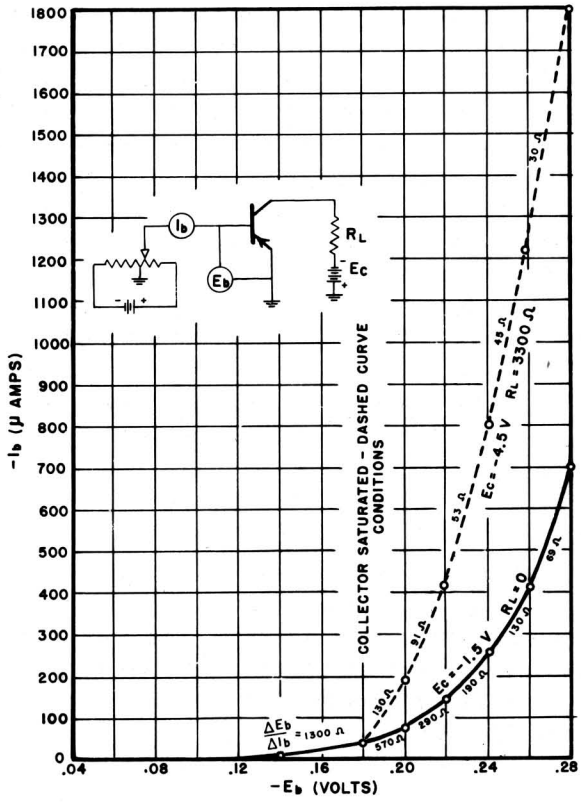

Fig. 10 - Input resistance of common emitter stage (SX-160 for saturated and unsaturated collector).

sync will be the average I_b divided by the duty factor of sync; this is about 12 I_b. Variations of I_s with signal level will be minimized by making E_s relatively large compared with the amplitude of sync applied to T_2. The primary effect of elevated temperature on T_2 is to increase the base current flow during sync as a result of increased I_{co} and I_{eo}. With an experimental SX-161 transistor (the n-p-n counterpart of the experimental SX-160) an induced change in I_s of 100 microamperes changed the output pulse width 0.5 microseconds. A similar increase in I_{co} and I_{eo} would have the same effect. The 2N35 exhibited a greater storage effect, the output pulse being widened 2 microseconds by the same change in I_s.

The two-transistor separator of Fig. 9, driven by the circuit of Fig. 7b, was connected to an RCA receiver. The sync output was applied to the balanced horizontal transistor phase detector described in *LB-914, A Symmetrical Transistor Phase Detector for Horizontal Synchronization*. An SX-160 and an SX-161 were used as T_1 and T_2 respectively. When the smaller values of C_1 and C_2 were used, for separation of horizontal sync only, the performance of the circuit was quite satisfactory. Sync held over the full range of usable signal levels and produced no shift in raster when the sync in the signal was reduced to 12 per cent. Transistor interchangeability was good and simulated increases of 100 microamperes in I_{co} and I_{eo} in both stages produced only minor changes in centering. When the larger values of C_1 and C_2 are used to permit separation of both horizontal and vertical sync, performance is similar except for the decrease in horizontal impulse noise immunity resulting from the longer time constants. This effect is discussed in a later section.

The circuit of Fig. 9 produces negative sync output which, as mentioned, is suitable for driving the transistor phase detector described in *LB-914*. The sync polarity may be reversed by operating T_1 as a common collector amplifier or by operating T_2 as a common emitter amplifier. Fig. 9 is presented as an example of a two-stage separator, and the discussion thereof explains some of the design factors involved. Many variations are possible. Since for each of the two stages there are three possible amplifier types (common emitter, base, or collector) two basic transistor types (p-n-p or n-p-n) and three means of biasing (self-base bias, self-emitter bias, or direct coupling), the number of possible combinations is in the hundreds. Many such combinations have obvious disadvantages, but many others would be workable circuits. Although it has not been possible to test all of these, the circuit of Fig. 9 is believed to be among the better two-stage separators.

One-Stage Sync Separators

The two functions of sync separation and sync clipping are usually performed by separate vacuum tubes in commercial television receivers. A two-stage transistor separator was discussed in the previous section. However, the sharp cut-off and saturation characteristics of the junction transistor make possible its use as a

one-stage separator, in which the same stage both separates and clips the sync pulses.

The one-stage separator is shown in Fig. 11. The bias developed by the emitter current flow through R_1 permits T_1 to conduct only during sync. At this time T_1 is driven to collector saturation, thus clipping the tops of sync as well as any noise that may be present. The output of T_1 is thus double clipped and will have a fixed output amplitude approximately equal to E_2. A one-stage separator can also be built with the self-bias elements R_1 and C_1 in the base circuit, but this has the disadvantage that collector leakage current I_{co} passes through the bias resistor.

There are certain differences in the self-biasing action between Fig. 11 and T_1 of Fig. 9. In Fig. 9, T_1 is not driven to saturation. The average collector current will thus vary with signal level. Since the collector current is the major component of the emitter current, it will cause adjustments in emitter bias with signal level. The change in base current required to produce a given change in bias current is low because of the base-to-emitter current gain of the transistor.

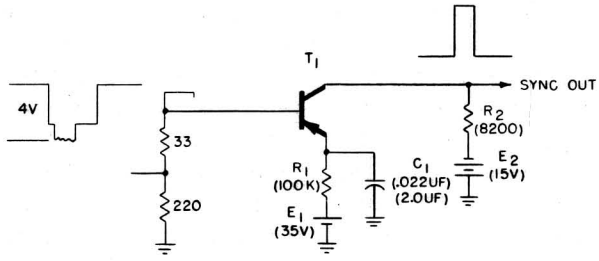

Fig. 11 - One stage sync separator.

In Fig. 11, since the collector is driven to saturation during sync at all signal levels, the collector current cannot increase with signal level. If the emitter bias is to adjust properly to varying signal levels, the adjustment must then come from changes in base-to-emitter current flow. As previously noted, after collector saturation, the base-emitter junction takes on the characteristic of a forwardly biased diode. The fall in input resistance beyond saturation is shown by the change in slope of the dotted curve of Fig. 10. The resistance falls well below 100 ohms. In this circuit the rectified input signal itself must provide the variations in bias, without benefit of the current gain of the transistor. The relationship between the required input signal level and source impedance and the variations encountered in signal amplitude and I_{eo} will be illustrated by an example. The separator circuit of Fig. 11, driven by the circuit of Fig. 7a, was installed in an RCA receiver. The source impedance to the separator was 250 ohms and the absolute level of sync tips varied from +1 to +4 volts above ground for maximum combined excursions of a-g-c control setting and signal strength. Since the emitter bias closely follows the level of sync tips, this means a 3-volt variation across R_1. This change in current through R_1 due to change in signal level will be called ΔI_S; in this case it is equal to 33 microamperes.

Let us allow a 50 microamperes variation in I_{eo} with temperature and unit to unit differences. Now equating ΔI_b, the maximum resultant variation in current charging C_1 during each sync pulse, to the variations in currents discharging C_1:

$$\Delta I_b = \Delta I_S + \Delta I_{eo} = 83 \text{ microamperes}$$

Dividing the above average value by the duty factor of sync to get the base current flowing during each sync pulse gives about 1 ma. The normal video input signal is about 4 volts across the 250-ohm load. Sync normally represents 1 volt of this signal, so that 4 ma of sync current flows in the source load. Since the input resistance of the transistor at saturation is very low, most of this current is available as input current to the transistor. Thus there is a safety factor to take care of weak signals or low percentage sync. The performance of the system under adverse signal conditions and normal temperature variations is good, but details will be given in the following section where a more refined version of the circuit is given. It may be noted here that increasing R_1 will decrease that part of ΔI_b due to signal level variations, but will not change the effect of temperature changes. If the allowance made for I_{eo} could be reduced, the signal source impedance could be raised.

It is also possible to build a common-base single-transistor separator as shown in Fig. 12. This arrangement produces a shorter rise-time than would be achieved with the same

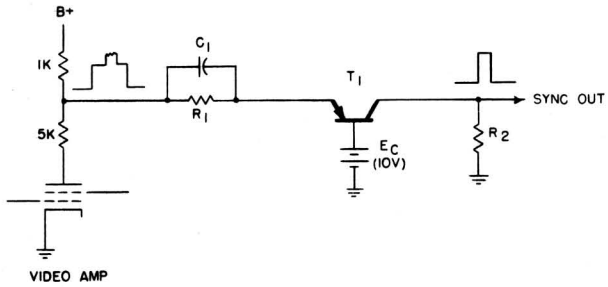

Fig. 12 - Common base one stage sync separator.

transistor operated with common emitter. The biasing action is very similar; however, since the video source must supply the sync output current directly, this circuit requires a greater video input current for proper separation.

Sync Separator Noise Immunity

The synchronizing ability of a television receiver in the presence of impulse noise is a function of the noise characteristics of both the sync and the a-g-c circuits. This discussion is devoted to the former. One characteristic of a sync separator which aids noise immunity is the ability to clip off noise so that it never exceeds the level of the sync output. The separators described in the previous sections do this. Another very important factor is that the separator not block or cut off for long periods following noise pulses. Impulse noise disturbances are normally of relatively short duration and low duty factor. The loss of sync information during the actual noise pulses usually does little harm. However, if the separator has long time constants that can charge on the noise pulses and keep the separator cut off for a long time thereafter, a serious loss of sync information results.

A long separation time constant is necessary for the separation of vertical sync. If horizontal sync is taken from the same circuit, the time constant must be on the order of 100 times that required for horizontal separation alone. This seriously affects horizontal noise immunity as shown by a comparison of lines 2 and 4 in Table I. One of the most effective solutions to the problem is the use of two separators, one optimized for horizontal and one for vertical. This represents an added expense, although the practicality of the one transistor separator makes it less so.

Another popular solution in vacuum tube circuits is the use of a double time constant in the grid circuit of the separator. The application of this principle to a transistor circuit is shown on Fig. 13.

In vacuum tube circuits the equivalent in the grid circuit of R_3, which is part of the

Table I

Comparative Sync Separator Noise Immunity

Sync Circuit	Minimum signal level giving good horizontal synchronization in presence of impulse noise	
	2V Detector Level	6V Detector Level
1. Standard RCA KCS-82 sync circuit (3 tube sections)	380 μv	200 μv
2. Fig. 11, one-stage transistor separator	3000	1200
3. Fig. 13, above with double time constant	800	250
4. Fig. 11 with C_1 = 0.022 μf for horiz. separation only	70	70
5. Fig. 14, transistor with diode controlled time-constant	300	200

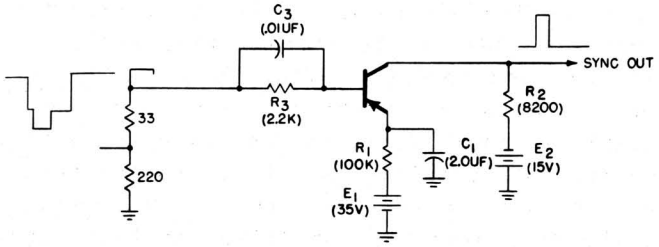

Fig. 13 - One stage separator with double time-constant.

short time constant combination, is made very large so that it limits the degree of charging possible in the large time constant circuit. The presence of this series resistance does not seriously reduce the tube gain to vertical sync because of the very high input resistance of the vacuum tube. The low input resistance of a transistor amplifier limits the usefulness of such a circuit.

In this case, R_3 reduces the separator gain to vertical sync, and hence must be restricted in value. The values shown in Fig. 13 reduced the vertical gain of the circuit by about one-half. Comparison of lines 2 and 3 shows about a 3 to 1 improvement in horizontal noise immunity.

The common channel separator circuit of Fig. 14 gives a marked improvement in noise immunity without appreciable loss in gain. This circuit is basically the common-emitter single-transistor separator previously described, adapted for positive power supply operation. However, it has two R-C time constant combinations in the emitter circuit which are brought into play at the proper time by diode D_1.

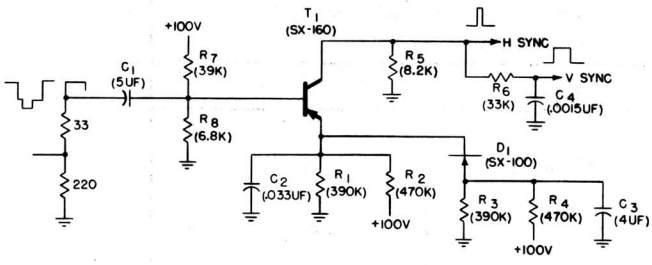

Fig. 14 - One stage sync separator with diode controlled time-constant.

During each sync pulse, the emitter current of T_1 biases D_1 in the forward direction, placing the long time constant of R_3-R_4-C_3 in the bias circuit. This will maintain the emitter bias for the duration of the vertical sync pulse, permitting its proper separation. Any noise pulses will also cause D_1 to conduct, charging C_3. However, after the noise pulse the excess charge on C_3 will keep D_1 open; and horizontal separation can resume as soon as the potential across the short time constant combination R_1-R_2-C_2 reaches the normal value. Comparison of lines 2 and 5 shows an average 8 to 1 improvement in horizontal noise immunity for the double time constant circuit.

Performance of One-Stage Sync Separator

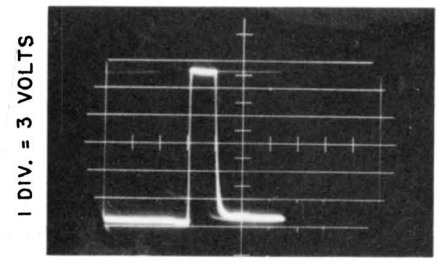

Fig. 15a - Horizontal rate.

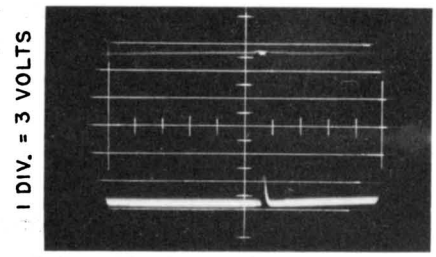

Fig. 15b - Field rate.

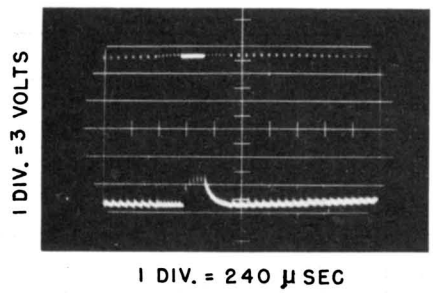

Fig. 15c - Expanded vert. sync.

Fig. 15 - Sync output waveforms (one transistor separator of Fig. 14 with off the air signal).

The one-stage separator with diode controlled time constant shown in Fig. 14, driven by the circuit of Fig. 7b, was temporarily installed in an RCA receiver and checked against commercial requirements. The results are summarized below. Those characteristics which cannot be expressed readily in absolute terms are given in terms of comparison with the normal KCS-82 sync separator.

Weak Signal Performance: The weakest intelligible signal is held in sync.

Sync Separation: No blanking appears in sync and no raster changes appear until sync is reduced below 15 per cent for most SX-160 transistors.

Output Waveform: 0.4 μsec rise-time, 1 μsec decay. (See Fig. 15).

Raster Straightness: No noticeable raster bends.

Impulse Noise: Vertical and horizontal synchronization comparable with the normal KCS-82. (See Table I).

Airplane Flutter: Withstands somewhat more severe flutter than KCS-82 circuit.

Transistor Interchangeability: Ten out of ten SX-160 transistors, selected for V_{ce}>30 volts, performed satisfactorily.

Temperature Effect: Three of the above transistors chosen at random were heated to 60°C without appreciable change in performance. The highest I_{eo} was 30 microamperes at 27°C and 80 microamperes at 60°C.

Line Voltage Tolerance: Good separation from 85 to 130 volts.

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