LB-952

A SILICON N-P-N JUNCTION TRANSISTOR BY THE ALLOY PROCESS

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Approved

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Introduction

Silicon has semiconductor properties very similar to those of germanium and in theory it can be used very much like germanium for the preparation of various types of transistor devices. The present almost exclusive use of germanium for these devices is largely a matter of convenience, since germanium is easier to work. A comparison of silicon characteristics with those of germanium shows that efforts to master silicon techniques may be amply rewarded through the advantages offered by silicon for high-temperature-device operation.

Silicon n-p-n alloy junction transistors have been prepared with satisfactory electrical performance, although most of the available silicon crystal material was not of the best quality. The attainable base-to-collector current amplification factor, α_{cb}, has been found to depend greatly upon the minority carrier lifetime of the silicon used. Average α_{cb} values of about 6 have been obtained with silicon having 2 microsecond lifetime; when improved silicon with 20 microsecond lifetime is used, α_{cb} values of over 100 have been obtained. Typical data, using 2 microsecond silicon, at collector conditions of 1 milliampere and 6 volts are: power gain = 34 db at 4 kc, 16 db at 300 kc and 6 db at 1 Mc; reverse current I_{co} at 6 volts = 0.1 microampere; noise factor = 23 db at 4 kc. The anticipated superiority of silicon over germanium at elevated temperatures has been observed. In one test, for instance, satisfactory electrical performance was obtained at 150 degrees C. At this temperature, saturation currents lower than 10 microamperes were observed.

General Discussion

It is appropriate to examine the published physical data on germanium and silicon, as of interest for transistor use. These data are assembled in Table I.

The higher energy gap of silicon leads to the presence in silicon of a far lower density of thermal carriers than in germanium, as shown in Table I. Since the uncontrollable fraction of the output current of a transistor is proportional to the thermal carrier density, it follows that this current is very much smaller in silicon than in germanium. This difference becomes particularly important at high operating temperatures. Calculations show, for instance, that at 150 degrees C, saturation current density values of 1.6 amp/cm^2 for germanium and 0.0007 amp/cm^2 for silicon, each with room-temperature resistivity of 2 ohm centimeters in the transistor range. One may predict, therefore, that at 150 degrees C and at a total collector area of 1 mm^2 that 16 milliamperes of the collector current would be independent of

Table I

Semiconductor Characteristics of Germanium and Silicon

Quantity	Germanium	Silicon	Reference
Energy Gap	0.75-0.0001 T volts	1.12-0.0003 T volts	J. Bardeen and W. Shockley, *Phys. Rev.*, 80, 72, 1950
Density of thermal carriers at 300°K	$2.5 \times 10^{13}/cm^2$	$6,8 \times 10^{10}/cm^2$	E. M. Conwell, *Proc. I.R.E.*, 40, 1329, 1952
Intrinsic resistivity at 300°K	47 ohm-cm	63,600 ohm-cm	E. M. Conwell, *Proc. I.R.E.*, 40, 1329, 1952
Donor ionization energy	0.01 volt	0.05 volt	G. L. Pearson and J. Bardeen, *Phys. Rev.*, 75, 865-883, (1949)
Acceptor ionization energy	0.01 volt	0.046 volt	G. L. Pearson and J. Bardeen *Phys. Rev.*, 75, 865-883 (1949) E. Burstein et al *J. Phys. Chem.*, 57, 849, 1953
Electron drift mobility at 300°K for 10 ohm-cm material	3900±100 cm^2/volt sec	1200±100 cm^2/volt sec	M. B. Prince, *Phys. Rev.*, 92, 681,1953 and *Phys. Rev.*, 93, 1204, 1953
Hole drift mobility at 300°K for 10 ohm-cm material	1900±50 cm^2/volt sec	500±50 cm^2/volt sec	M. B. Prince, *Phys. Rev.*, 92, 681, 1953 and *Phys. Rev.*, 93, 1204, 1953

emitter voltage when the base material is germanium, while only a few microamperes of the collector current need be uncontrollable when the base material is silicon. Although in practice the currents may be somewhat higher, the ratio is still significant.

In view of the above, silicon may be preferable to germanium in transistors designed for applications where high operating temperature and low uncontrolled collector current are important considerations. In some of these applications high frequency response may not be essential so that the lower mobilities of holes and electrons in silicon are not a serious disadvantage.

As a first step to investigate the advantages offered by silicon for high temperature operation, a low-power, audio frequency silicon transistor has been developed and is the subject of the present bulletin.

Method of Fabrication

General methods involved in the preparation of alloy transistors have been described in *LB-868*[1] and here only the variations in technique necessitated by the use of silicon in place of germanium will be described. P-type silicon of 2.0 - 4.0 ohm-cm resistivity, grown as a single crystal, generally in the 111 direction, is used. Transistor theory indicates that material of high lifetime preferably greater than 20 microseconds is necessary for good transistor results. However, much of the work in the early stages was done with silicon of lower quality.

Alloying Materials

The dot materials used to form the junctions were selected after extensive tests in which the metallurgical as well as the electrical nature of alloy junctions in silicon were investigated. A variety of n-type impurity elements and dilutants were tested. As in the case of the n-p-n germanium transistors,[2] the use of dilutants was found to minimize the introduction of thermal mismatch strains in the neighborhood of the junction. Also, the use of

[1] *LB-868, Germanium P-N-P Junction Transistors.*

[2] See *LB-903, A Germanium N-P-N Alloy Junction Transistor,* for detailed discussion of this problem.

suitable dilutants in the dot material was found valuable in promoting wetting and liquefaction of the silicon during the alloying process. When pure antimony is used in forming a junction, wetting is difficult to attain and intersolubility of the elements is very low even at 900 degrees C. When gold is added to antimony, wetting and solubility are good even at temperatures as low as 500 degrees C.

As an outcome of these tests, an alloy of 25 wt. per cent of antimony in gold was chosen for emitter dot and one of 36 and 2 wt. per cent respectively of gold and arsenic in lead was chosen for collector dot. Thermal mismatch is appreciable when the gold-antimony eutectic is used but due to the small size of the emitter dot a relatively strain-free junction is obtained. In case of the larger collector dot, less thermal mismatch can be tolerated and consequently the gold-arsenic-lead alloy is used. This alloy is less brittle and has a lower melting point than the gold-antimony eutectic and consequently, leads to a more strain-free junction. This junction, however, does not appear to be as efficient an injector of minority carriers as does the gold-antimony eutectic junction and consequently gold-arsenic-lead alloy is not used for emitters.

The gold and arsenic of the collector dot are both donors. The gold, however, produces donor levels only 0.33 volt above the occupied band in silicon.[3] It therefore does not contribute to the formation of a n-type region in the p-type silicon. The arsenic, on the other hand, produces donor levels 0.05 volt below the bottom of the conduction band and converts the recrystallized silicon to high conductivity n-type material. Though more gold than arsenic is present in the collector dot, the converse is true of the recrystallized silicon. The distribution coefficient of gold in silicon is very small and consequently only a very small percentage of the gold is caught in the recrystallizing silicon.

The two alloys discussed above are brittle and consequently difficult to form into disk-shaped dots. This problem is solved, in case of the gold-antimony eutectic, by using spherical rather than disk-shaped emitters. These spheres are made rather simply by crushing the alloy into particles of appropriate size and by heating these in an inert gas to about 600 degrees C. At this temperature the particles melt and as a result of surface tension assume a spherical form. A sphere diameter of approximately 16 mils is used. In the case of the collector dot, the brittleness problem is solved by making the dot from a disk of gold superimposed upon a disk of lead-arsenic alloy. Dots of this type can readily be punched out from a strip of gold and a strip of lead-arsenic alloy bonded together. A gold thickness of 5 mils, a lead-arsenic alloy thickness of 12 mils and a disk diameter of 40 mils are used.

A third dot is used for securing ohmic contact to the base wafer. This dot is made of 10 wt. per cent copper in indium in the form of a disk 35 mils in diameter and 12 mils thick.

Processing

The silicon base wafer used for the transistor is ground to a thickness of 10 mils and then etched to 5 mils. A suitable etching solution is:

70 per cent Nitric Acid	80 parts
52 per cent Hydrofluoric Acid	50 parts
99½ per cent Glacial Acetic Acid	50 parts
Bromine	1 part

Before the dots are applied to the silicon surface for alloying, they are rinsed in 52 per cent hydrofluoric acid. This rinse leads to the formation of a fluorine-containing salt film on the dot surface which serves as a flux in promoting effective wetting during the alloying process. The three dots are alloyed onto the silicon in one firing step. A graphite boat and graphite washers are used as described in *LB-868*[1], the base wafer and the dots being assembled as shown in Fig. 1. After loading, the assembly jig is fired in a dry mixture of

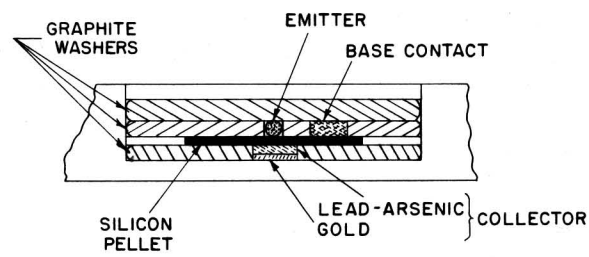

Fig. 1 – Silicon transistor parts assembled for alloying.

[3] Taft and Horn, *Phys. Rev.*, Vol. 93, p. 64, (1954).

hydrogen (10%) and nitrogen (90%) for 2 minutes at 800 degrees C. After cooling at a rate of 250 degrees C per minute, the transistor is etched for one minute in a hot sodium hydroxide solution. Good results are obtained with a solution of 7 grams of the hydroxide in 100 cc of water heated to 80 degrees C.

The etch suggested above was chosen on the basis of a series of tests in which the reverse characteristics of the junction and the recombination velocity of the minority carriers in the surface adjacent to the junction were measured after various surface treatments. The evaluation of the surface recombination rate was comparative rather than absolute. An effective lifetime determined by bulk as well as surface recombination was measured by a pulse injection technique described in *LB-934*.[4] Changes observed in this effective lifetime due to surface treatments of the diode were then attributed to variations in the rate of surface recombination. Results obtained indicated that the surface recombination velocity characteristic of the diodes tested was generally high and also that it was greatly affected by surface treatments. The effective lifetime value for a particular diode was found to increase as much as by a factor of five, as a result of the sodium hydroxide etch referred to above. Increases in effective lifetime was also found to result from the conventional etching techniques used with germanium but these increases were lower in magnitude. Rough, absolute measurements of the surface recombination velocity made on special samples of silicon showed qualitative agreement with the diode measurements. Recombination velocities varying from 7000 to 800 cm/sec depending upon surface conditions have been observed.

After etching, the silicon transistors were mounted on glass bases and encapsulated in plastic or alternatively were mounted on metal bases and hermetically sealed into metal cans with surrounds of either air, helium or vacuum. The 84X-40 white potting compound and the 90X-3 activator of the N. Stanley Chemical Co. are used for plastic encapsulation. This potting compound is room-temperature setting and required 18 hours for hardening.

[4] *LB-934, Measurement of Minority Carrier Lifetime and Surface Effects in Junction Devices.*

Electrical Characteristics

In course of the experimental work with silicon transistors, more than 100 units have been tested for electrical characteristics and performance. A few units have exhibited electrical performance roughly comparable with that of germanium p-n-p alloy units; for these, collector-to-base current amplification factor (α_{cb}) of 110 and power gain of 40 db have been obtained. Values as low as 6 and 30 db respectively, however, have been more common due primarily to the use of silicon of short lifetime. Data presented below do not represent the best units prepared but the characteristics of units typical of recent lots made. These transistors have been prepared with 2 - 3 ohm-cm silicon having a bulk minority carrier lifetime of 2 microseconds.

Measurements have been made at room temperature and also in a range from 30 degrees C to 150 degrees C. The upper limit is not imposed by the silicon but by solder used in mounting and encapsulation. The measurements have been of three types. The first type has been concerned with the determination of hybrid π-equivalent common emitter circuit parameters[5]; the second, with the determination of static characteristics and the third type, with the evaluation of small signal operating characteristics such as power gain, current gain, and noise factor.

Room-Temperature Measurements

The range of values of hybrid π-equivalent common emitter circuit parameters (Fig. 2) measured on a group of transistors are shown in Table II.

For comparative purposes, a range of values for the TA-153 p-n-p germanium transistor is included.

The range of values of base to collector current amplification factor, α_{cb}, power gain and noise factor measured for the same group of transistors are shown in Table III.

[5] *LB-915, A P-N-P Triode Alloy Junction Transistor for Radio Frequency Amplification.*

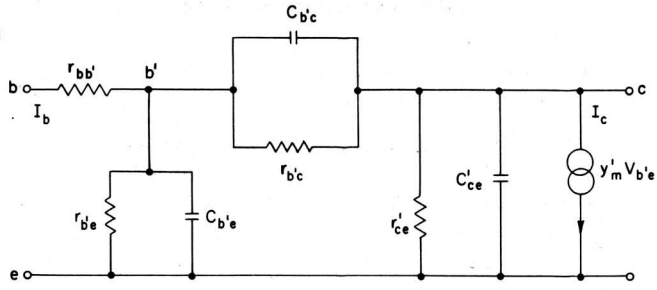

Fig. 2 - Single-generator base-input hybrid π-equivalent circuit.

Table II

Hybrid π-Equivalent Circuit Common Emitter Parameters of Silicon Transistor Measured at $E_c = +6$ volts, $I_E = 1$ ma

Parameter	Range of Values	Approx. TA-153 p-n-p range
$r_{bb'}$ ohms	100-300	200-500
$r_{b'e}$ ohms	100-300	600-2000
$C_{b'e}$ μμf	3200-9000	10,000-25,000
$r_{b'c}$ megohms	0.3-1.2	2
$C_{b'c}$ μμf	74-129	35
W mils (Note 1)	0.7-1.4	1-3

Note 1 - W is the base-layer thickness and is calculated from

$$C_{b'e} = \frac{q}{kT}\frac{W^2 I_E}{2D}$$

Table III

Gain and Noise-Factor Values of Silicon Transistor

	Range	Approx. TA-153 Range
4 kc Current amplification factor (α_{cb})	3.6-13.0	20-100
4 kc Power gain db	23.4-34.0	35-48
300 kc Power gain	9.2-14.2	0-10
1 kc Noise factor	14-29	15-25

All values of gain measured at $V_C = 6v$, $I_E = 1$ ma. Power gains measured with resistive input and conjugate matched output. Noise factor measured at $E_C = -1v$, $I_E = 1$ ma.

Room temperature static output characteristics of one of the transistors are shown by the curves labeled A on Fig. 3.

The data presented in the above tables and curves highlight the great similarity of germanium and silicon transistors with regard to room-temperature performance. The tendency towards lower current amplification factor, α_{cb}, of the silicon units is perhaps the greatest point of difference. This tendency emphasizes the greater difficulty involved in achieving high surface and bulk lifetime of minority carriers in silicon than in germanium. Because the base layer thickness was a little smaller for the silicon units no material inferiority in frequency response is observed with silicon in this comparison.

Measurements at Elevated Temperatures

Transistors hermetically sealed with helium in metal cans were found most stable at high temperature. This type of transistor was used, therefore, for measurements at elevated temperatures.

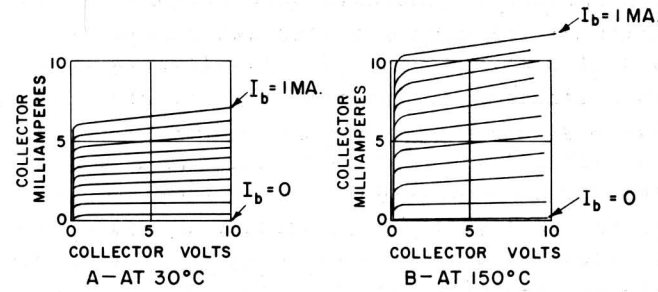

Fig. 3 - Output characteristics of a silicon transistor (base current I_b in ten equal steps from 0 to 1 ma).

The curves labeled B in Fig. 3 show static output characteristics at 150 degrees C of the same silicon transistors for which the curves labeled A show room-temperature results. These characteristics, contrary to findings with germanium, show an increase in α_{cb} with temperature. They also show evidence of the very low reverse current expected with silicon. A plot of this current to the 1-mm diameter collector dot is shown in Fig. 4. The reverse current apparently contains a surface leakage component as well as the saturation current, yet at 150 degrees C it is far less than the reverse current obtained with germanium at the same temperature.

The base-emitter bias required for a 1-ma emitter current in a silicon transistor is shown as a function of temperature by curve A

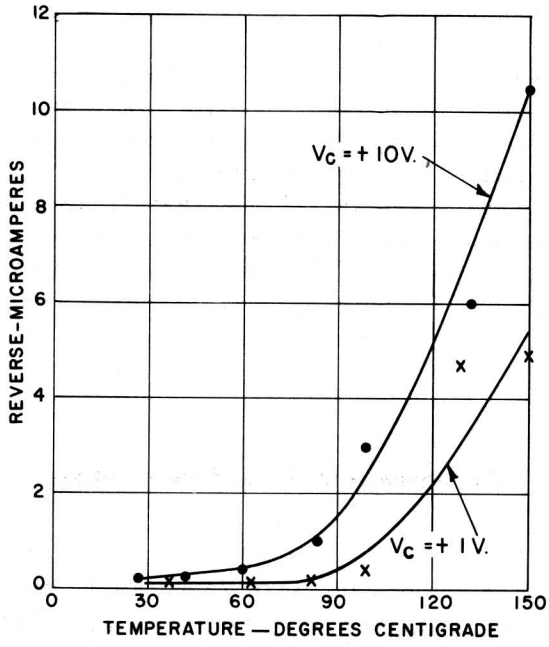

Fig. 4 - Reverse current as a function of temperature.

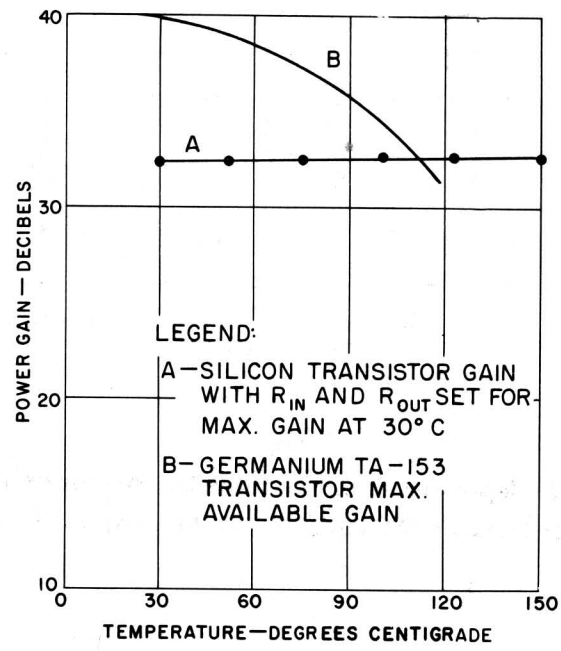

Fig. 6 - Power gain versus temperature.

of Fig. 5. Curve B shows comparative data for a p-n-p germanium transistor. That a larger bias is required for the silicon transistor follows directly from a consideration of the diode equation

$$I = I_s \left[\exp\left(\frac{eV}{kT}\right) - 1\right].$$

The value of the saturation current, I_s, is about six orders of magnitude less for silicon than for germanium and consequently a larger bias voltage is required with the silicon transistor for the same forward current flow. The voltage, V, across the junction required for any particular forward current flow decreases with temperature even though the above expression indicates the opposite trend. This is true since I_s increases more rapidly with temperature than the term "$\exp\left(\frac{eV}{kT}\right)$" decreases. The greater decrease in base-emitter bias with temperature noted for germanium is, however, largely due to an increase in saturation current flow through $r_{bb'}$. The voltage drop across $r_{bb'}$ is in a direction to increase the forward voltage at the p-n junction and calls for a component of bucking voltage in the base-emitter bias.

The variation of power gain of a silicon transistor with temperature is shown in Fig. 6. Curve A shows the power gain with input and output impedance set for maximum power gain at 30 degrees C. For comparison, the maximum available power gain for a germanium transistor is shown by curve B in the same Fig. The measurements were made at V_C = 6 volts and I_E = 1 milliampere.

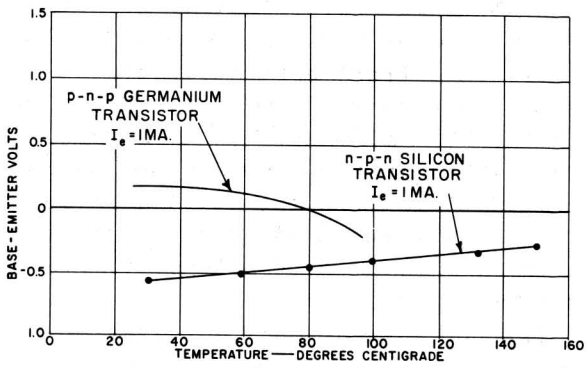

Fig. 5 - Base-emitter bias for constant emitter current as a function of temperature.

Conclusions

Silicon techniques have been mastered to the extent that transistors capable of as much as 30-40 db gain are achieved. The performance of these transistors at elevated temperatures has been found to accord with expectations. Present variability in results, however, do indicate the need for further work devoted particularly towards the improvement of crystal growing procedure, surface etching treatments and encapsulation techniques.

Herbert Nelson