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LB-924

A DELAY EQUALIZER FOR COLOR TELEVISION

RADIO CORPORATION OF AMERICA

RCA LABORATORIES DIVISION

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Approved

Stuart Wm Seeley

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Introduction

Faithful reproduction of an image in color or black-and-white requires uniform amplitude and delay responses throughout the useful video frequency band. Delay distortion introduced by the i-f amplifier of the receiver near the high-frequency cutoff may be substantially equalized by an appropriate equalizer inserted in the video input of the transmitter. This bulletin describes a four-section all-pass phase equalizer having a characteristic which closely matches the NTSC Delay Specification of July 21, 1953.

General Description of the Delay Equalizer

The NTSC has specified curve (a) in Fig. 1 as the required equalization for the cutoff delay of the average color receiver. This characteristic becomes the relative video delay of the transmitter and all associated terminal equipment including the equalizer. Established tolerances are indicated by dotted lines.

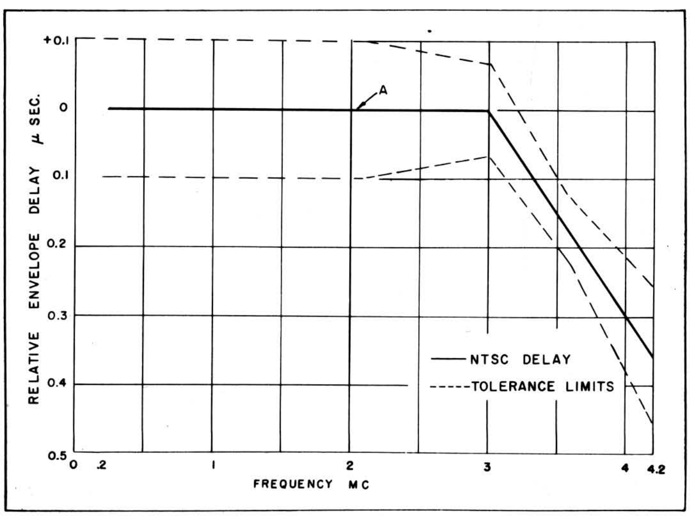

Fig. I - NTSC specifications of envelope delay.

An equalizer having an envelope delay characteristic closely approximating this NTSC Specification is shown in Fig. 2. Circuit constants and other constructional data are given in Table I.

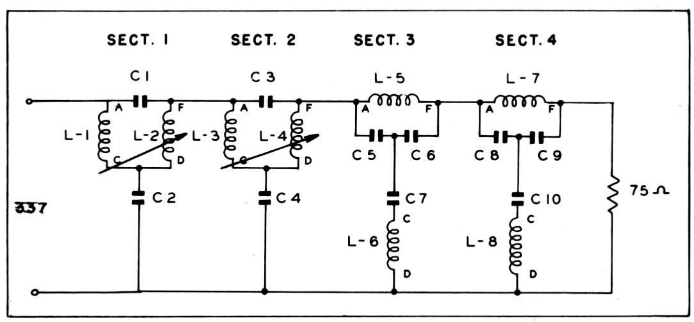

Fig. 2 - Cutoff delay equalizer.

A large number of designs are possible but all are not equally economical. In general, the designs that yield a delay no better than the tolerances imposed on the equalizer are the most economical. In this instance a tolerance equal to 15 per cent of the system tolerance specified in Fig. 1 appears to be appropriate in view of the overall system tolerances (except at the discontinuity at 3 Mc). Since each section is an all-pass type the amplitude response is theoretically 100 per cent at all frequencies when incidental dissipation is not considered. The constant resistance feature of the filter permits direct termination of coaxial cables limited only in practice by incidental reflections in the filter due to dissipation, distributed capacitance and imperfections in line-up. Fig. 3 shows the theoretical envelope delay of the filter and the delays of the

Table I

CONSTRUCTIONAL DATA FOR EQUALIZER

Section	Element	Inductance (μh)	O.D. of form (in.)	Number of turns	Coupling	Capacitance (μμf)
1	L_1	11.0	1/2	36-3/4	L_1 and L_2 overlapped approx. ¼" series aiding inductance 33.7 μh	
	L_2	11.0	5/8	29		
	C_1					468
	C_2					5980
2	L_3	5.87	1/2	23-1/2	L_3 and L_4 spaced approx. 5/16" series aiding inductance 12.9 μh	
	L_4	5.87	5/8	19		
	C_3					468
	C_4					2300
3	L_5	5.82	1/2	19	No coupling	
	L_6	2.63	1/2	10		
	C_5					935
	C_6					935
	C_7					2300
4	L_7	4.68	1/2	14	No coupling	
	L_8	2.29	1/2	9		
	C_8					831
	C_9					831
	C_{10}					1709

All coils are close wound with #28 heavy formex.

Coil Form – A. L. Hyde Co., I Main St., Greyloch, N. J. order #254937-II

Shield Can – National Co. type RZ.

individual sections. Submultiples of the total delay cannot be obtained at intersection junctions on account of the staggered design.

The pole and zero pattern of the filter shown in Fig. 4 will be recognized as an application of the "condenser plate" analogy in the potential analogy method of equalizer design. Poles and zeros of all-pass sections have quadrantal symmetry in the complex frequency plane. The remote pair of poles and zeros depart somewhat from the regular spacing of critical points so that a better approximation to the desired envelope delay characteristic is obtained.

Construction of the Delay Equalizer

The values of all inductors and capacitors should lie within ±1 per cent of the theoretical values given in Table I. Accuracy of this order is not difficult to achieve if ordinary laboratory standards are available. All capacitors

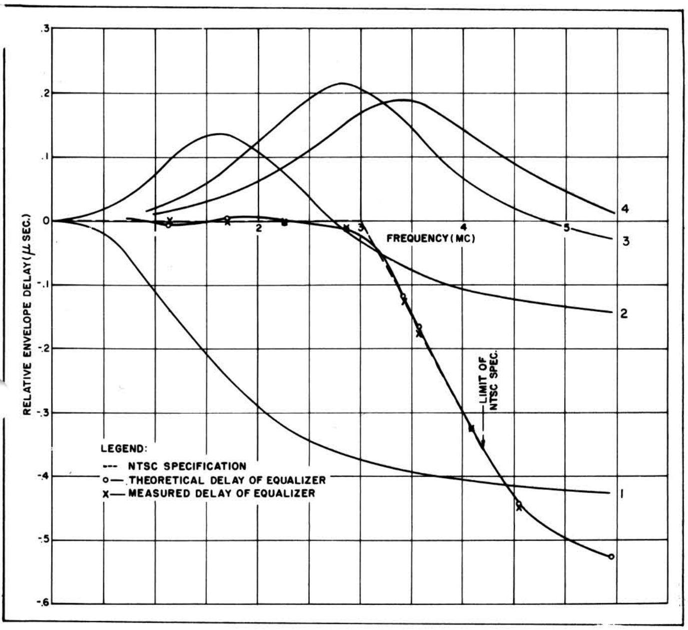

Fig. 3 – Envelope delay characteristic of equalizer.

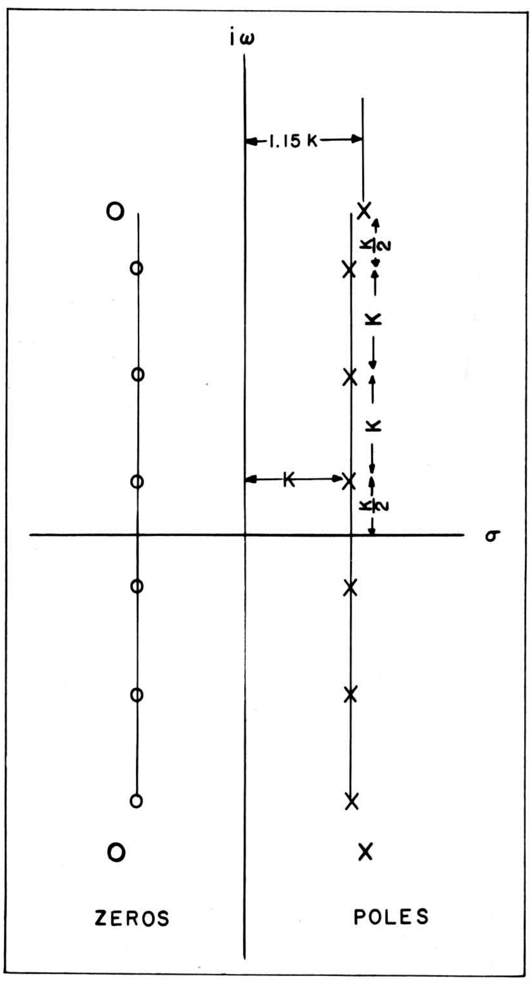

Fig. 4 – Pole and zero pattern of delay equalizer.

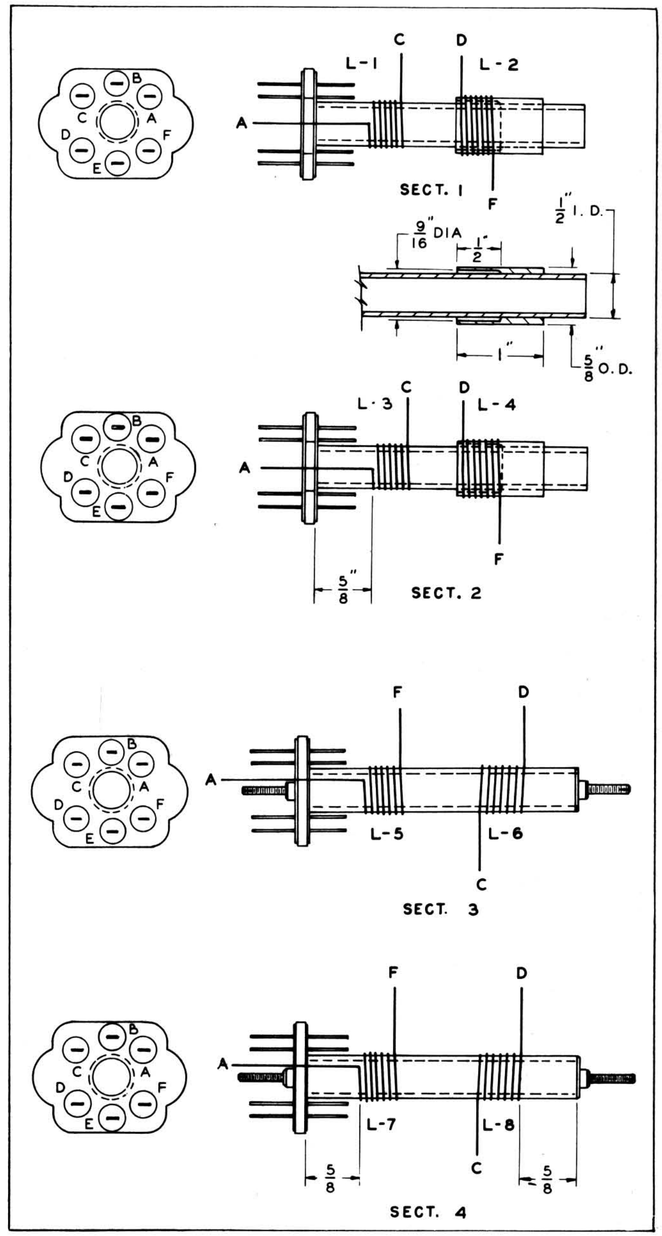

Fig. 5 – Coil details. See Table I for coil data.

should be measured on a standard bridge. Inductors in sections 3 and 4 do not involve mutual coupling and may be adjusted in the short circuit and open circuit tests described below without previous measurement. Inductors in sections 1 and 2 do involve coupling and must be measured on a standard bridge or by some equally accurate means. Resonance of an inductor with a large calibrated capacitor (0.0015 μf or so) in a parallel circuit at an accurately known frequency is an acceptable technique.

Inductors in sections 1 and 2 are measured first without coupling and then connected series aiding for adjustment of the coupling that results in the correct overall inductance given in Table I.

Fig. 5 shows details of coil winding.

Short Circuit and Open Circuit Tests

Short circuit and open circuit tests should be made on each section of the equalizer as a check on the element values. Fig. 6 illustrates the variation of the input impedance as a function of frequency for the two conditions. Frequencies that correspond to zero impedance and infinite (theoretically) impedance may be compared with the values listed in Table II.

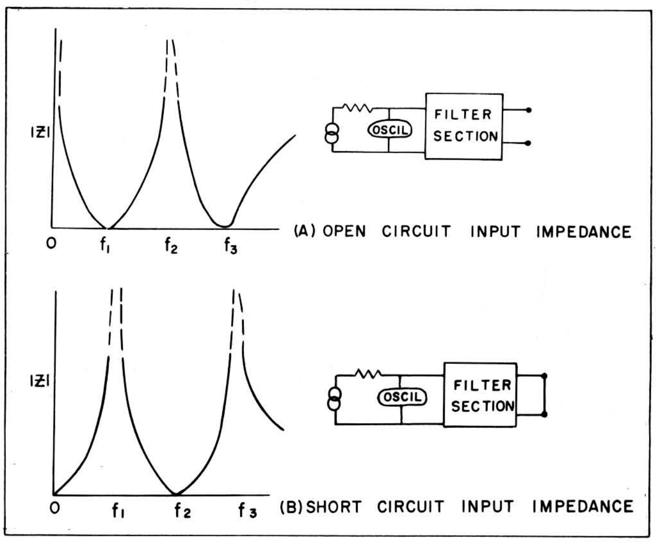

Fig. 6 - Open and short circuit input impedances of delay equalizer.

Table II

OPEN AND SHORT CIRCUIT TEST FREQUENCIES			
Section	f_1	f_2 (megacycles)	f_3
1	0.563	1.27	2.84
2	1.21	2.05	3.48
3	2.13	3.06	4.41
4	2:57	3.65	5.20

Since there is no mutual coupling in sections 3 and 4 the inductors L_5 and L_7 may be adjusted to give the section "infinite" impedance at a frequency f_2 for the open circuit condition or "zero" impedance at the same frequency for the short circuit condition. The remaining inductors L_6 and L_8 then are adjusted for "zero" impedance at the frequency f_1 in the open circuit condition or "infinite" impedance at the same frequency in the short-circuit condition. Confusion may result in using the short circuit and open circuit criteria for inductance setting if the initial values of inductance are too far off.

Test for Reflections

Another check on the accuracy of construction of the equalizer is the observation of reflections by means of a frequency sweep and an oscilloscope connected across the input end. The input envelope should theoretically be flat. In an actual filter ripples of ± 5 per cent are probably tolerable and it is possible that larger reflections may not unduly disturb the envelope delay of the complete equalizer. There is a temptation to flatten the input envelope by touching up the element values in the completed filter. This may sometimes be accomplished with success, especially if the individual sections are disconnected and observed separately for reflections.

Test Results on an Experimental Equalizer

The envelope delay ($d\varphi/d\omega$) of an experimental equalizer as measured by phase sweep apparatus described in LB-883, *A Sweep Method For Measuring Envelope Delay*, is shown in Fig. 3. This sweeper measures the delay of the envelope formed by two variable video frequencies which are separated by a constant frequency difference of 200 kc. When a comparison is made with the NTSC curve and the theoretical curve for the equalizer, it is permissible to shift curves vertically for the best agreement. The deviation of the data

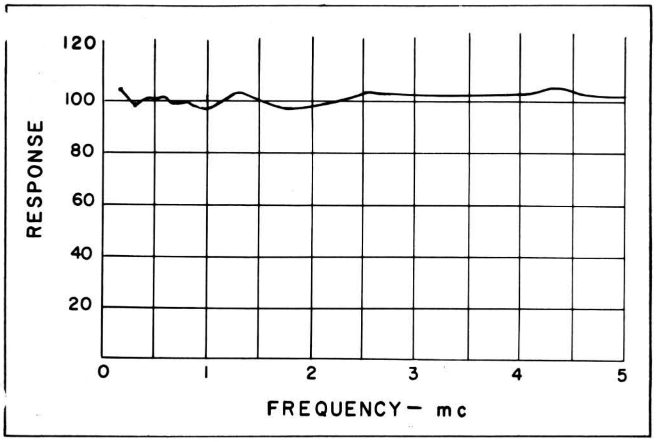

Fig. 7 – Amplitude response of equalizer.

points from the NTSC Specification is approximately ±0.015 microsecond except at the discontinuity at 3 Mc deviation from the theoretical curve is approximately ±0.01 microsecond.

Element values were not changed from the measured values in obtaining the amplitude response curve shown in Fig. 7. Some "touching up" of values would probably diminish the maximum deviations ±5 per cent. However, losses in the equalizer limit the performance unless account is taken of finite Q values in the design itself.

G. L. Fredendall