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LB-914

A SYMMETRICAL TRANSISTOR PHASE DETECTOR FOR HORIZONTAL SYNCHRONIZATION

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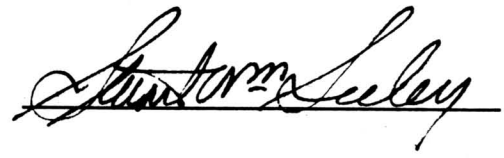
Approved



A Symmetrical Transistor Phase Detector for Horizontal Synchronization

Introduction

This bulletin describes the application of the developmental type TA-211 symmetrical transistor as a balanced phase detector for controlling the horizontal oscillator of a television receiver. While the circuit used is basically similar to that described in earlier bulletins,[1,2] it has been refined to obtain a high degree of balance and uniformity of performance under unfavorable conditions of transistor symmetry and temperature.

The transistor phase detector was used to control a stabilized multivibrator type of horizontal oscillator[3] having a sensitivity of approximately 150 cps per volt. Approximately ten volts of single-ended sawtooth and thirty volts of single-ended sync were required to produce a pull-in of 120 to 180 cps.

Wide variations in the absolute values of transistor parameters and in the degree of symmetry resulted in less than 0.5-volt unbalance in the absence of sync. Laboratory measurements indicated that the performance was relatively unaffected by temperatures up to 55 degrees C (130 degrees F). These results were obtained with transistors having values of r_c, I_{co}, and α_{cb} which varied as much as 3:1 when the collector-emitter roles were interchanged.

Symmetrical transistors are constructed in the same way as conventional junction transistors with the exception that the collector and emitter junctions are made identical. The circuit was tested with two varieties of symmetrical transistors. One had both junctions similar in size to the normal emitter junction in the developmental type TA-153; the other had both junctions similar to the collector junction. Both varieties of transistors performed equally well.

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[1] LB-906, *Symmetrical Properties of Transistors and Their Application.*

[2] LB-907, *A Study of Transistor Circuits for Television Receivers.*

[3] A typical circuit of this oscillator and its associated a-f-c filter is given in LB-761, *A Novel Ten-Inch Television Receiver.*

Comparison of the Transistor and Diode Phase Detector

The transistor phase detector may be compared with a conventional double-diode phase detector. As shown in Fig. 1, both circuits provide an error voltage which is positive or negative, depending upon whether the sync pulse arrives before or after the center of the sawtooth retrace interval. In the double-diode phase detector, this desirable balanced characteristic is obtained by peak rectification of the composite sync-sawtooth voltages applied to each of the diodes, and by subtracting these two peak voltages to produce the required error voltage. In the transistor circuit, a similar

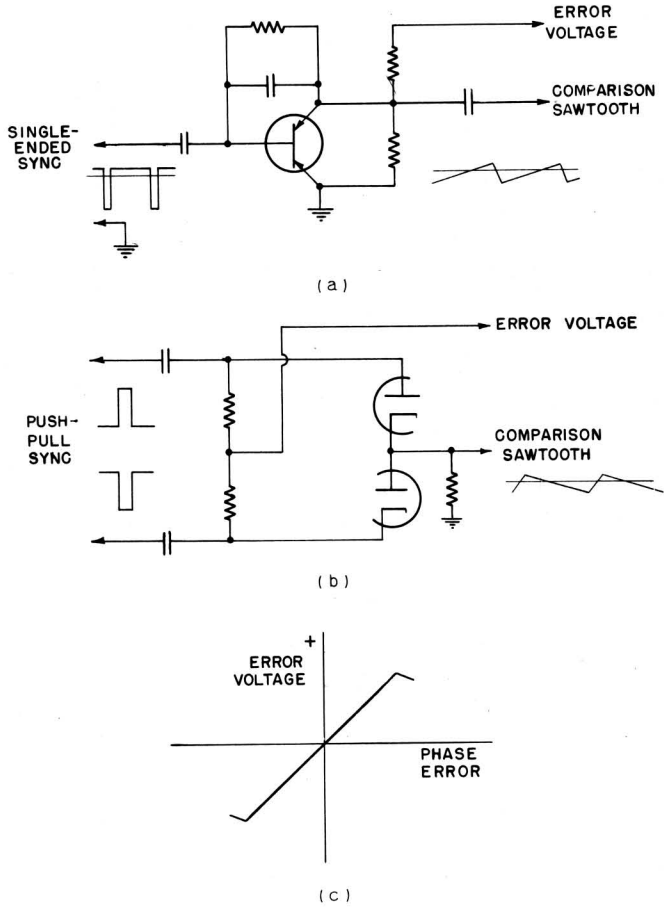


Fig. 1 - Comparison of (a) symmetrical transistor phase detector, and (b) conventional double diode phase detector. The corresponding control characteristic is shown in (c).

characteristic is obtained by making use of the symmetrical property of the transistor, i.e., the ability of the transistor to conduct in either direction, as shown by the family of curves in Fig. 2. By gating the transistor on with the sync pulse, the sawtooth coupling capacitor is charged toward the instantaneous voltage of the sawtooth during the sync pulse interval; this produces an error voltage across the sawtooth coupling capacitor which depends on the relative phase of the sync and sawtooth.

For both the transistor and the diode phase detector, the error voltage is relatively insensitive to the amplitude of the sync signal as long as the peak-to-peak value of the sync exceeds the peak-to-peak sawtooth. In addition, both detectors are balanced so that random noise does not contribute to the d-c output of the detectors. In the absence of sync, as when switching between channels, the control voltage of both detectors remains relatively unchanged so that the oscillator continues to run synchronously.

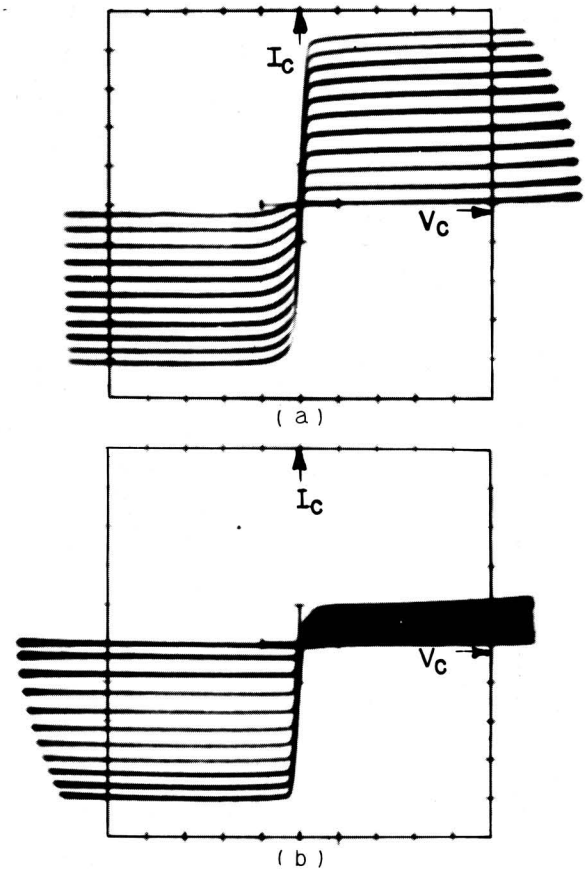


Fig. 2 - Collector current curves for (a) symmetrical and (b) asymmetrical transistors, for constant base current.

Transistor Phase Detector

A basic transistor phase detector circuit is shown in Fig. 3. Because of transistor symmetry, two arrows are used to designate the fact that either element can serve as the emitter or the collector, depending upon the applied potentials. Either element is therefore referred to as a "collector-emitter". The operation of the circuit depends on the transistor conducting only when the sync pulses are present. Thus, if the instantaneous sawtooth voltage on the collector-emitter is positive at the instant the sync pulse "gates" the base, the transistor conducts and produces a negative error voltage across C_2; if the phase is such that the collector-emitter is negative, C_2 is charged to produce a positive error voltage. In this way, the transistor acts as a bidirectional switch charging C_2 to essentially the instantaneous sawtooth potential at the time of sync arrival.

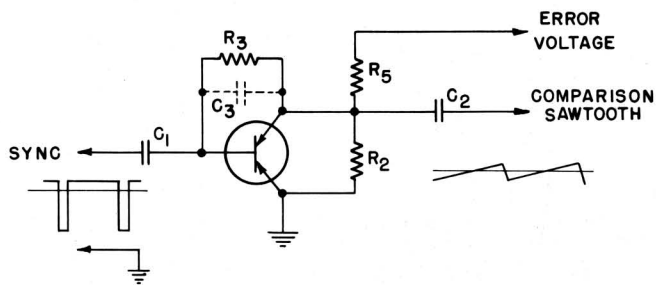


Fig. 3 - Basic transistor phase detector circuit.

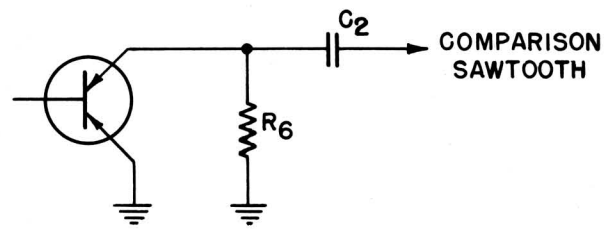
Since it is essential for the transistor to be cut off between sync pulses, capacitive coupling of the sync is used to permit the equivalent diode formed by the base and the collector-emitter to clamp the sync peaks to ground. For the transistor to be cut off between sync pulses, the base voltage during this interval must remain more positive than the peak positive collector-emitter voltage; i.e., the peak-to-peak sync voltage at the base must exceed the peak-to-peak sawtooth.

Normal operation also requires that the collector current during the sync interval be sufficiently large to charge the sawtooth coupling capacitor to the instantaneous voltage of the sawtooth during the sync interval. The amount of collector current which flows during the sync interval is dependent primarily on the amount of base current, and thus primarily on the back impedance of the base. As some transistors have too high a back base impedance, shunting a resistor R_3 from the base to the collector is necessary to provide sufficient base and collector current.

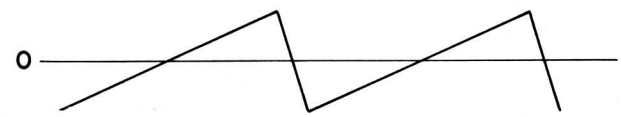
Balance Considerations

When a constant-current generator is used to supply the sync, removing the sync is equivalent to floating the base. If the transistor capacitances to ground are neglected, any net charge developed across the sawtooth coupling capacitor is then due to transistor asymmetry. The resultant polarity of this unbalance voltage reverses when the transistor collector-emitter roles are reversed.

The voltage at the base in the absence of sync, when the base impedance to ground is high, is shown in Fig. 4. This waveform may be understood by noting that the base-to-emitter voltage must be approximately zero over the sawtooth cycle. Thus, during the negative part of the sawtooth when the grounded electrode is the emitter, the base voltage is approximately zero; during the positive part of the sawtooth, when the ungrounded electrode is the emitter, the base-to-ground voltage is approximately the same as the positive part of the sawtooth.



(a) Transistor circuit



(b) Collector-emitter voltage

(c) Base-to-ground voltage

Fig. 4 - Waveforms in the absence of sync when the base circuit impedance is high.

In the absence of sync the transistor will be turned on by the base current resulting from the capacitance between base and ground. Transistor non-linearity results in the corresponding collector current developing an error voltage. As the base driving impedance is increased by reducing the driving capacitor, the resulting unbalance decreases. However, a small base driving capacitor results in compression of the sync signal at the base, so that a larger sync amplitude is required to cut off the transistor between sync pulses.

The addition of capacitor C_3, shown dotted in Fig. 3, permits the use of a large sync coupling capacitor while maintaining balance. This is accomplished by providing equal base currents over each half of the sawtooth cycle. Since the base-to-emitter voltage is approximately zero, C_3 causes a base current, during the time that the sawtooth is negative, that is similar to the base current through C_1 during the time that the sawtooth is positive. Therefore when C_1 is approximately equal to C_3, it is possible to supply the sync through a large capacitor and still maintain balance. As the sync at the base is now approximately one-half of the applied sync, the required minimum peak-to-peak sync voltage is twice the peak-to-peak sawtooth. The values of C_1 and C_3 are limited by the capacitance which their series combination shunts across the sync source impedance. Too large a value integrates the leading edge of the sync pulse and results in excessive picture shift with respect to the raster.

Temperature Effects

One of the effects of increasing temperature is the reduction of the output impedance of the transistor under cut-off conditions. To prevent distortion of the sawtooth, and consequent phase shift of the picture with respect

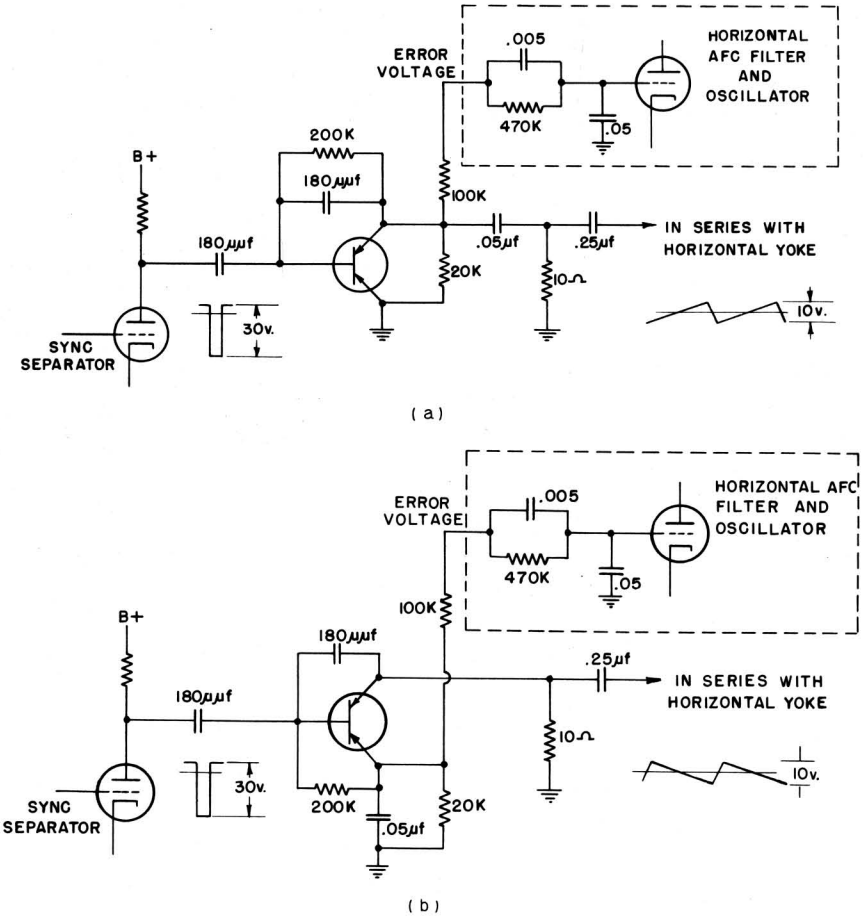


Fig. 5 - Phase detector circuits which operate with either polarity of comparison sawtooth.

to the raster, a low sawtooth driving impedance and a relatively large sawtooth coupling capacitor C_2 are necessary. Resistor R_2 is connected between the collector-emitter and ground in order to provide the proper time constant for the automatic frequency control loop.

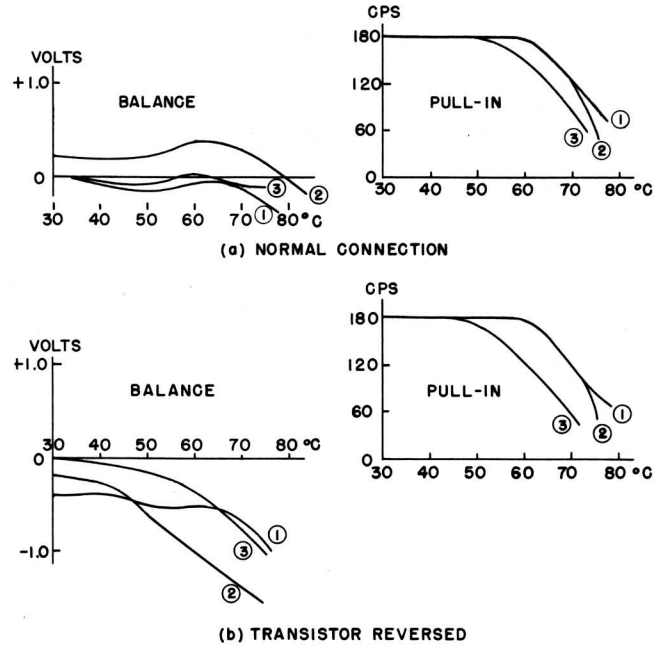
Another effect of increasing temperature is the reduction of the back base impedance. This produces excessive sync crushing at the base, as a result of which the sync amplitude becomes insufficient to cut off the transistor between sync pulses. To avoid this, either the amount of sync can be increased or the sync driving impedance can be lowered.

Circuit Details

Fig. 5 shows the transistor phase detector applied to representative receiver circuits. While the basic operation of each circuit shown is the same, the appropriate circuit must be used in conjunction with the proper sawtooth polarity in order to obtain the correct sense of oscillator control. Both circuits require negative sync which is available with conventional circuitry.

Ten volts of sawtooth were supplied to the transistor from a low-impedance source by placing 10 ohms between the horizontal yoke blocking capacitor and ground. This method provides a linear low-impedance sawtooth source, the phase of which accurately represents the beam deflection. Thirty volts of negative sync were supplied directly from the sync separator output.

Fig. 6 shows the circuit performance with a typical developmental TA-211 symmetrical transistor, and with two asymmetrical transistors. For most of the TA-211 units tested, the unbalance was under half a volt. All of the units, however, provided a pull-in of 120 to 180 cps that was relatively unaffected by temperature up to 55 degrees C (130 degrees F). Above this temperature the performance was limited by compression of the sync signal at the base. The possible effects of operation at elevated temperatures for extended periods were not investigated.



TRANSISTOR PARAMETERS						
Unit	α_{ce}	α_{cb}	r_b ohms	r_c Megohms	I_{co} @ -10v ma	Comments
1	.950	19	280 Ω	.440	.02	Typical
	.947	17	230 Ω	.218	.03	
	.986	68	530 Ω	.660	.02	Abnormal α_{cb} asymmetry
2	.966	28	550 Ω	.685	.02	
	.960	23	470 Ω	1.17	.02	Abnormal r_c asymmetry
3	.955	21	340 Ω	.40	.04	

Fig. 6 – Effect of variation of transistor parameters on balance and pull-in. The two sets of values given for each transistor correspond to the reversal of the emitter and collector roles.

The amount of sync compression in the circuit of Fig. 6 can be decreased by further reducing the sync driving impedance, as shown in Fig. 7. This is accomplished by increasing

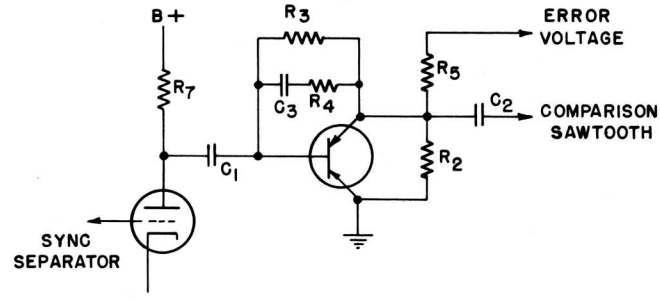


Fig. 7 – Balance is obtained by adding a resistor R_4 approximately equal to the sync source impedance.

the capacitance of C_1. Balance is restored by similarly increasing C_3 and by adding a resistor R_4 in series with C_3 so that the balance is maintained as a result of the equality of the sync driving resistance and the resistance R_4. Since the driving resistance is the parallel combination of the sync output tube r_p and the sync output load resistance R_7, it is necessary to make R_7 small in comparison with r_p in order that the balance not be affected by variations in r_p. This places a greater burden on the sync separator than is present in the circuit of Fig. 5.

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