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LB-907

A STUDY OF TRANSISTOR CIRCUITS FOR TELEVISION RECEIVERS

RADIO CORPORATION OF AMERICA

RCA LABORATORIES DIVISION

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A Study of Transistor Circuits for Television Receivers

Approved

Stuart Wm Seeley.

Introduction

This bulletin describes a general study of transistors in television receivers. For this purpose, the development of a completely transistorized television receiver was undertaken. An experimental model using 37 transistors and a 5-inch kinescope, housed in a plastic cabinet 13 x 12 x 7 inches, was constructed. This portable receiver operates on a single channel using a self-contained loop, and has a total battery-power consumption of 13 watts, more than 25 per cent of which is consumed by the kinescope heater.

The development of a complete experimental receiver, even with a number of compromises, provided an opportunity to deal with the problems found in every stage and circuit of the receiver. Although experimental point-contact transistors have recently been developed which will provide oscillations for the entire v-h-f television band, considerable difficulty was found in providing wide-band r-f gain using transistors at these frequencies. This problem was much less difficult at intermediate frequencies and at the intercarrier-sound frequency. The second-detector problem of obtaining high rectification efficiency with low load impedances was solved by using a transistor detector. The video amplifier problem was complicated by the requirement for a high input impedance; however, with a combination of junction and contact transistors a stable, high gain video amplifier with a relatively high input impedance was built. An audio system using complementary symmetrical junction transistors was designed to produce high output with good efficiency.

In the synchronization and deflection portion of the receiver circuits were devised for using transistors in ways which differ from the analogues of amplifier tubes. A single transistor was used as a d-c setter, sync separator and sync amplifier. A simple and reliable horizontal a-f-c system was developed by utilizing the symmetrical properties of transistors. Point-contact transistors were found to be particularly economical pulse and sawtooth oscillators. The complementary symmetry principle was used to provide vertical deflection with high linearity and efficiency. In the horizontal deflection circuits, the fast high-current switching ability of transistors was used advantageously. An efficient circuit using the symmetrical property of the transistor, which has no analogue in electron tubes, was devised for horizontal deflection.

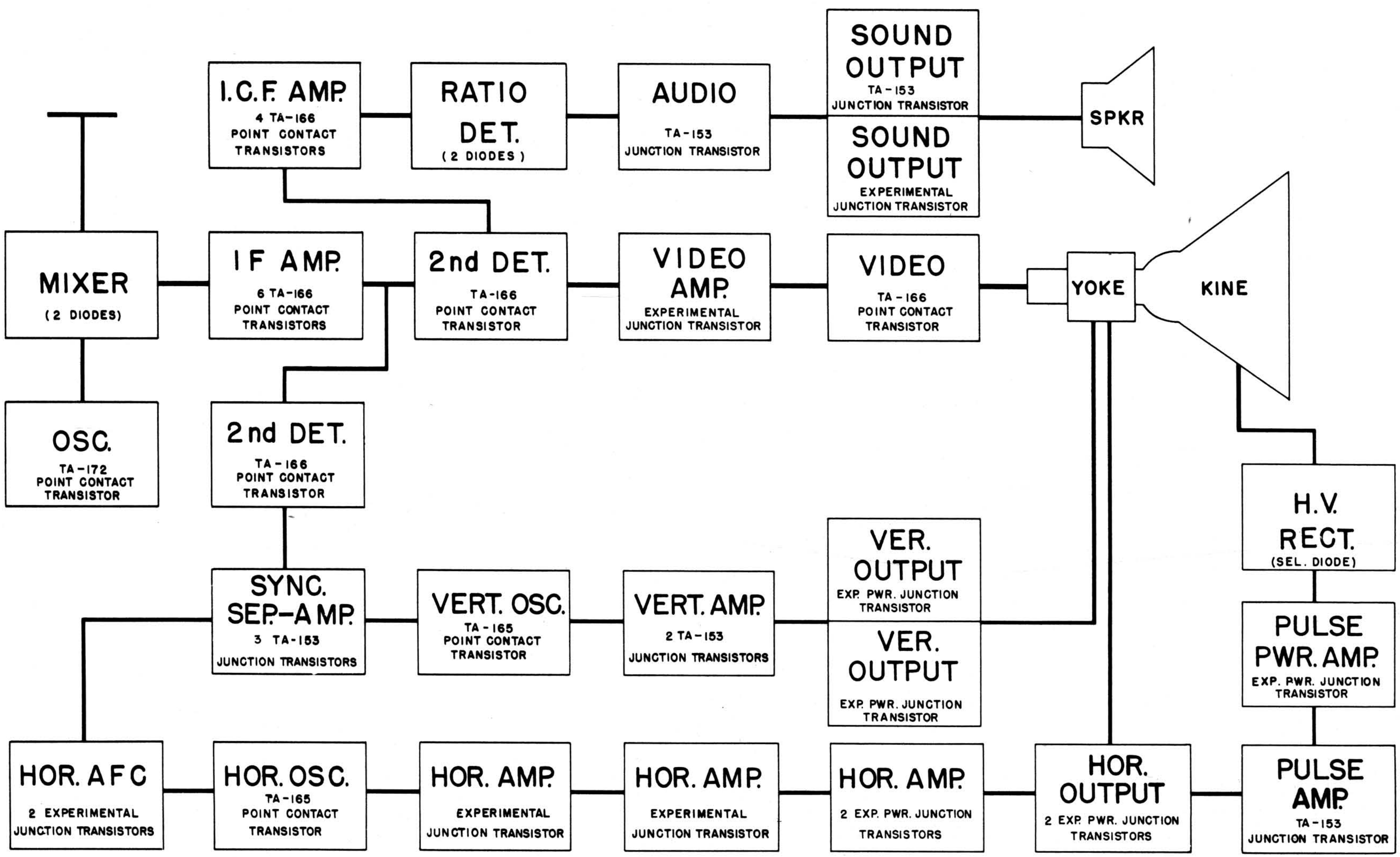


Fig. 1 – Block diagram of an experimental transistorized television receiver.

Signal Channel

The first part of this bulletin treats the signal channel consisting of the mixer, the intermediate-frequency amplifiers, the second detector, the sound channel and the video amplifier. The second part treats the deflection channel including the synchronizing and deflection circuits and the high voltage generator. A block diagram of the receiver is shown in Fig. 1.

at a break in the loop at the middle of the front side. To provide a means of impedance matching to the mixer diodes, a coil is used in shunt with the loop and tuning capacity. The combination of the loop and coil have an inductance of approximately one-half microhenry allowing a larger minimum tuning capacity. Optimum power transfer to the mixer diodes is achieved by connecting the diodes to balanced taps at an intermediate impedance point on the coil.

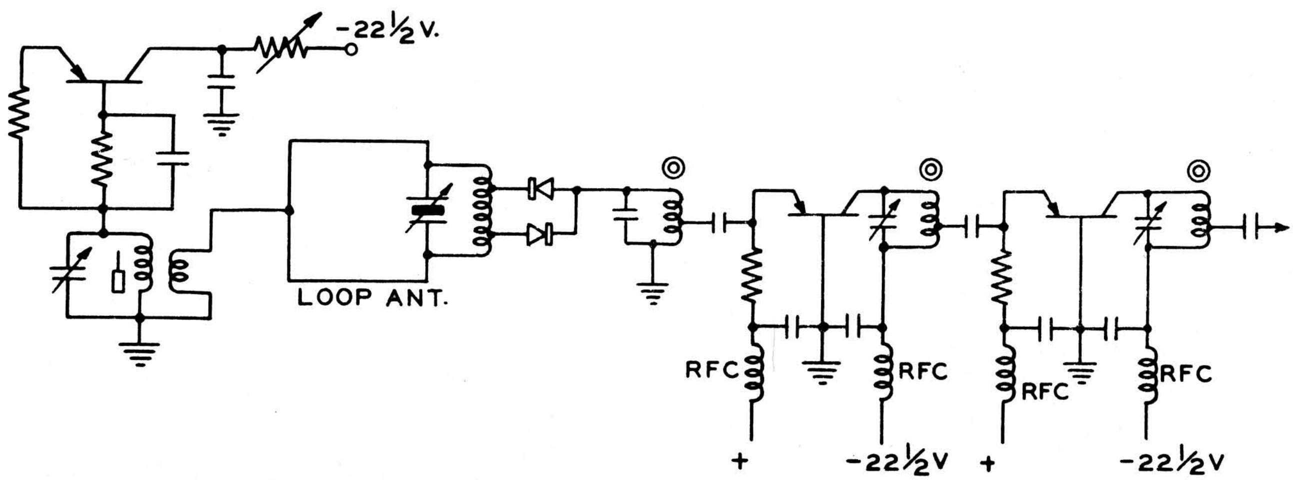


Fig. 2 - Schematic of local oscillator, mixer, and first IF amplifier.

The signal is picked up by a loop antenna, mixed with the local oscillator in a pair of crystal diodes, and the resulting difference signal amplified by six stages of grounded-base point-contact transistors. Two second detectors provide independent signals for the sync and video amplifiers. Intercarrier sound from the video second detector is amplified by four intercarrier frequency stages and demodulated by a ratio detector. The resulting audio signal is applied to an emitter follower stage driving a complementary type push-pull output stage.[1]

The video signal is amplified by a system combining the higher input impedance of a grounded emitter junction transistor with the high-frequency response of a point-contact type.

The tuned loop antenna was decided upon after a comparison of various antenna types which could be included in a case only 12 x 13 x 7 inches. The tuning capacitor is located

The local oscillator employs a type TA-172 point-contact transistor designed for high-frequency oscillator use.[2] The oscillator circuit provides a signal at 60 Mc for mixing with the Channel 4 carrier of 67.25 Mc. The local oscillator signal is coupled to the midpoint of the loop by a two-turn pickup coil wound over the oscillator tank.

The mixer circuit consists of two 1N54A crystal diodes in a balanced arrangement as shown in Fig. 2. The difference frequency is impedance matched to the first i-f amplifier by a tuned circuit which has a tapped coil. This 50-microhenry coil is wound on a ferrite toroid. By the use of the ferrite toroids for all coils in the tuned i-f stages, the effect of stray magnetic fields is reduced and shielding problems minimized. Large impedance transformation ratios are easily obtained because of

[1] LB-906, *Symmetrical Properties of Transistors and Their Application.*

[2] LB-867, *The Control of Frequency Response and Stability of Point-Contact Transistors.*

the high coupling coefficient obtainable. With a total diode mixer current of 1 milliampere the mixer circuit gain is -6 db or a 2 to 1 loss of signal voltage.

For simplicity the i-f amplifiers are stagger tuned. Each of the i-f amplifier stages consists of a point-contact transistor, type TA-166, operated in a grounded-base circuit. The collector of one stage is matched to the succeeding stage by a tapped coil similar to that previously mentioned. Collector voltage is supplied by a 22½-volt battery common to the entire receiver but decoupled by an L-C filter in each collector circuit. No attempt was made to keep the impedance of the collector circuit high outside of the bandpass as the type TA-166 transistors are short-circuit stable. The emitter bias was fixed at approximately 1 milliampere and supplied by a penlite cell battery. The photograph of one of the i-f stages in Fig. 3 shows the ferrite toroid used in the interstage tuned circuits.

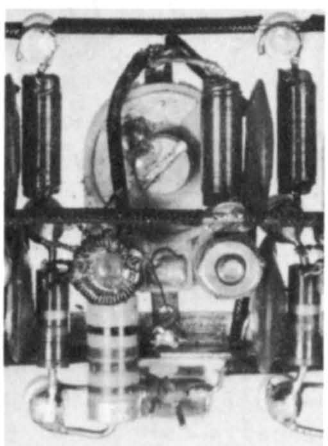


Fig. 3 - Close-up of ferrite toroid coil in i-f stage.

Overall power gain of the six stages and the second detector in the band pass shown in Fig. 4 is 47 db. The markers shown are at 5 Mc and 10 Mc showing the rising characteristic between 6.5 and 7.5 Mc and the flat top between 7.5 and 9.5 Mc.

The second detector presented a problem because of the relatively low input impedance of the video amplifier. The first proposal was a crystal detector, but because of the low impedances involved, the rectification efficiency was extremely low. Severe negative peak clipping occurred since the a-c load resistance was comparable or even less than the d-c load of the crystal rectifier. The logical step was to use a transistor as the detector.

The last i-f transformer is different from the preceding ones in that it has two windings and is double tuned. The second winding is tapped and feeds the emitter of the detector transistor, a point-contact type TA-166. This transistor does not have any bias applied to its emitter, the low side of the secondary winding being connected to ground. The emitter-base electrodes in the transistor act as a crystal rectifier, the resulting rectified signal appears in the collector circuit amplified by the current gain of the transistor.

Since the rectified signal is internally coupled to an amplifying part of the circuit there is no problem of keeping the d-c load resistance small in respect to the a-c load and hence negative peak clipping problems are avoided and a resulting improvement in rectifier efficiency is obtained. The collector load impedance was kept small to avoid the effects of the frequency-dependent input impedance of the video amplifier.

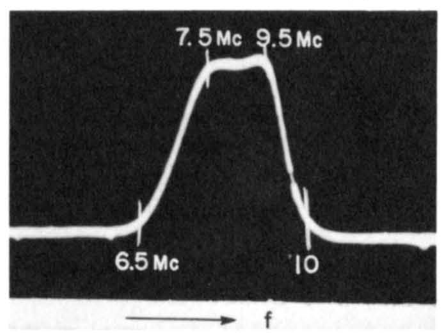


Fig. 4 - Frequency response of video amplifier.

The video amplifier was one of the first units of the receiver built and consequently was completed before other parts of the receiver were started. This presented the problem of building an amplifier to work from an unknown source impedance. Since junction transistors which could serve as video amplifiers were not then available, it was necessary to use a point-contact type of transistor in the amplifier to get sufficient high-frequency response. Unfortunately, point-contact transistors are most successfully used in a grounded-base circuit in which they have very low input impedance. To overcome this problem of low input impedance, a selected junction transistor was used in a base input circuit to drive the emitter of a point-contact unit as shown in Fig. 5.

The low-frequency voltage gain of the amplifier is 20 and the video response is shown in Fig. 6. The response of the basic amplifier with no equalization is shown in (a). The addition of a conventional video peaking coil (L_3) in the collector circuit of the contact unit alters the response as shown in (b). Further equalization is accomplished by the degenerative feedback provided by the resistance (R_1) in the emitter of the junction unit (c). The high output impedance of the junction unit permits the use of positive feedback in the base of the point-contact unit and the effect of this feedback provided by R_2 and L_2 is shown in (d). The result of bypassing R_1 at 1 Mc with a low-Q series resonant circuit is illustrated in (e). In all photographs the marker is at 2 Mc and the source impedance of the input signal generator is 1000 ohms.

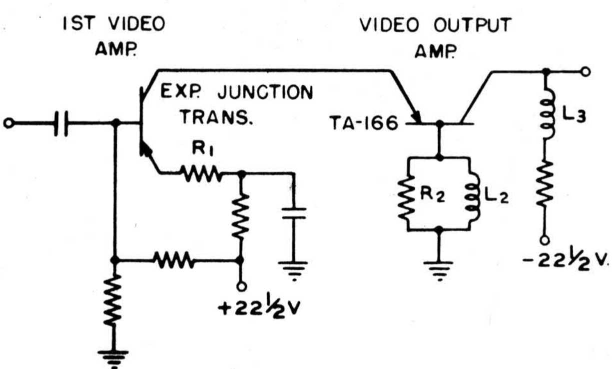


Fig. 5 - Video amplifier.

The use of a point-contact transistor in the output stage limited the voltage swing obtainable consistent with good frequency response and limited power dissipation. With the 2700-ohm load resistance used, the bias was adjusted to allow an 8-volt peak-to-peak swing in the output, since previous measurements had shown that this value was adequate to provide good picture contrast. However, in later operation of the amplifier it was found desirable to utilize all of this allowable swing for actual picture signal and consequently the sync pulses were permitted to drive the amplifier into the saturation region.

Because of this sync crushing it was necessary to provide a separate sync amplifier. To prevent this amplifier from loading the second detector excessively, a separate second detector was provided. This detector, which is similar to the video detector, is fed from a lower impedance tap on the driving transformer, thereby taking less of the available signal power. The sync amplifier is described later in connection with the deflection circuits.

A sound take-off trap is located in the video-detector circuit and provides the intercarrier-sound signal which is amplified by four stages tuned to the intercarrier frequency, 4.5 Mc. The first three of these stages are similar to the picture amplifier stage except that they are not stagger tuned, but peaked to 4.5 Mc. The fourth stage drives a standard ratio-detector transformer modified to operate from a lower source impedance. The demodulator has a peak separation of 120 kc and gives an audio output signal on the order of a volt.

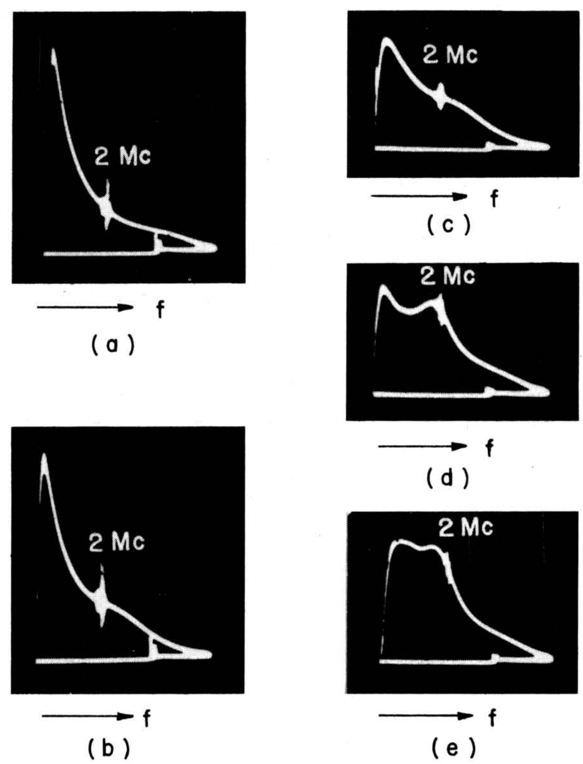


Fig. 6 - Frequency response of video amplifier.

This signal is amplified by a system of unusual design. An emitter follower circuit is used to drive a combination of a p-n-p and n-p-n transistor in the output circuit. This combination utilizes the complementary symmetry properties described in LB-906[1].

Deflection and Synchronization

The deflection and synchronization circuits are described in the following sections in the order in which they were developed, rather than in the order shown on the block diagram. This procedure is followed to indicate the manner in which the several circuits were evolved.

Vertical Deflection

The equivalent circuit of the vertical yoke consists of a resistance of 65 ohms in series with an inductance of 45 mh. A peak-to-peak current of 100 ma is required to deflect the beam three inches--the proposed picture height. Fig. 7 shows the ideal waveforms necessary to obtain linear deflection.

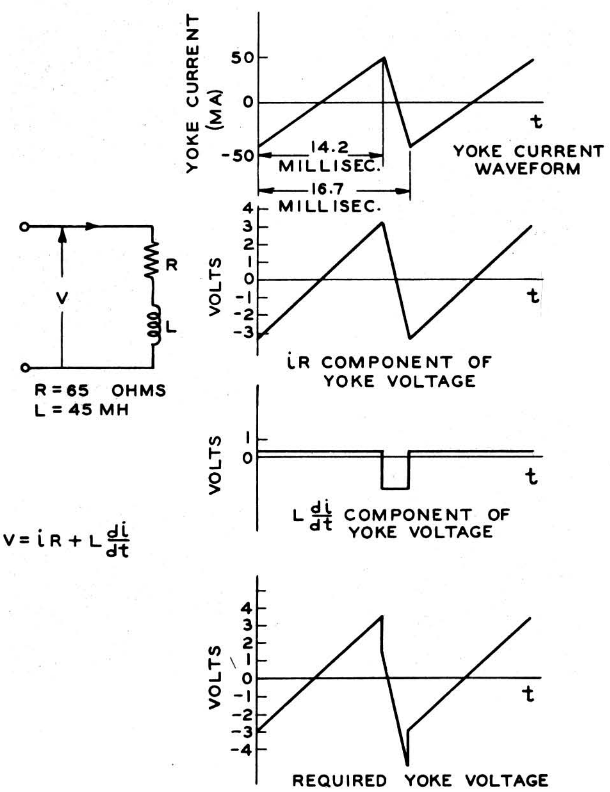


Fig. 7 - Theoretical vertical yoke waveforms

The waveform to energize the yoke is obtained from a synchronized relaxation oscillator using one TA-165 point-contact transistor. The operation of this circuit may be briefly described with reference to the simplified schematic shown in Fig. 8. The application of voltage causes the base of the transistor to assume a negative potential equal to the product of the base resistor, R_3, and the leakage current across the collector rectifying contact. (Appendix A)

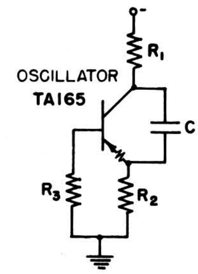


Fig. 8 - Vertical oscillator.

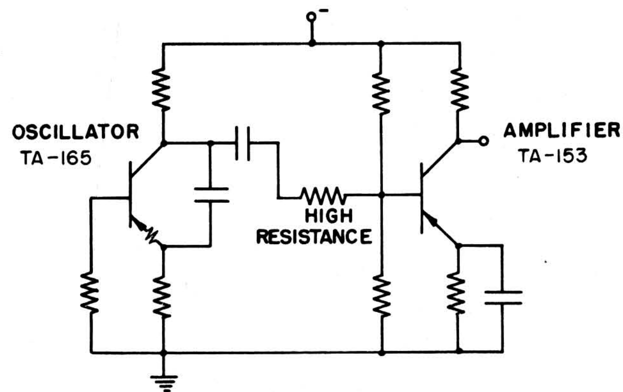
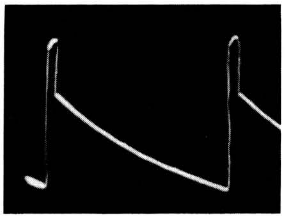
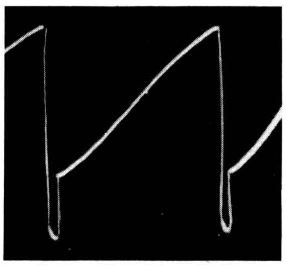


Fig. 9 - Vertical oscillator and amplifier circuit.

The emitter voltage is also negative because of the current which flows through R_2 to charge the capacitor, C. As long as the emitter is more negative than the base, the conduction through the emitter-collector path of the transistor is negligible. As the capacitor becomes charged, however, the leakage current increases while the charging current through R_2 falls off exponentially. Eventually a point is reached when the emitter is positive with respect to the base. The capacitor then begins to discharge through the emitter-collector path. Since the current gain of the transistor is greater than unity, the base current increases faster than the emitter current and the action becomes self-sustaining and continues until the capacitor is discharged. The cycle is then repeated. Synchronization is accomplished by applying positive pulses to the emitter at a rate somewhat faster than the free-running rate. The voltage waveform across R_1 is shown in Fig. 10a. The ratio of sawtooth to pulse may be altered by changing the ratio of the collector resistance to the emitter resistance.



(a) Vertical oscillator output



(b) Vertical yoke voltage

Fig. 10 - Waveforms.

In coupling the oscillator to a transistor amplifier, it is necessary to meet two conditions if the amplifier output is to be an undistorted replica of the generated waveform:

(1) The loading effect of the amplifier on the oscillator must be negligible.

(2) The amplifier must be fed from a current rather than a voltage source.

The first of these arises because of the reactive output impedance of the oscillator. Any loading of the oscillator therefore not only attenuates the output but also alters the shape of the waveform. The second condition is imposed because of the non-linear input impedance of the transistor amplifier. Equal increments of collector current are generated by equal increments of base current, which, because of the non-linear input impedance of the transistor, do not correspond to equal increments in base voltage.

The two conditions are met by using high-resistance coupling as shown in Fig. 9. This resistance prevents loading of the oscillator and at the same time approximates a constant current source for the amplifier.

Fig. 11 shows the three-stage vertical amplifier. The first stage consists of a grounded-emitter stabilized class A amplifier using a TA-153 junction transistor. The second stage is a grounded collector power junction transistor which provides the necessary drive at low impedance to operate the output stage. Frequency selective feedback, provided by R_1 and C_1 serves to compensate for distortion introduced by the first two stages. The output stage consists of a grounded-collector complementary-symmetrical push-pull amplifier using both a p-n-p and an n-p-n transistor.

This type of amplifier permits direct coupling to the vertical yoke without the presence of de-centering current. The Class-A efficiency obtained with this circuit was 24 per cent, which compares favorably with the

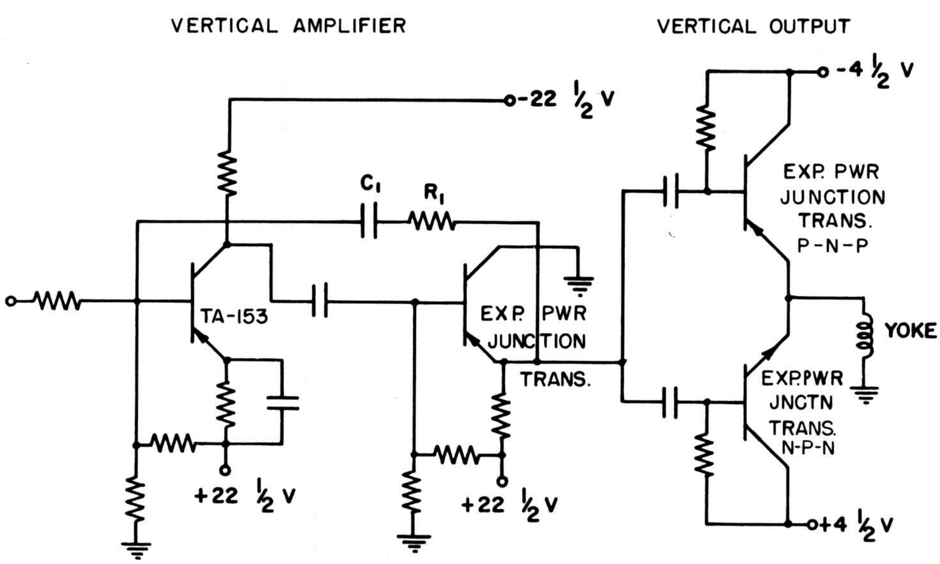
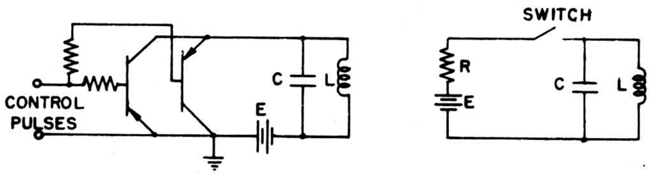


Fig. 11 - Vertical amplifier

maximum theoretically possible value of 33 per cent (for a sawtooth wave). The voltage waveform across the yoke is shown in Fig. 10b.

Horizontal Deflection

The operation of the horizontal-deflection system is based on the fact that linear bi-directional currents may be made to flow in an inductive yoke if a source of energy is periodically connected and disconnected with a fast switch.[1] An investigation of such a system is included in Appendix B and the results of this investigation are tabulated in Fig. 12.



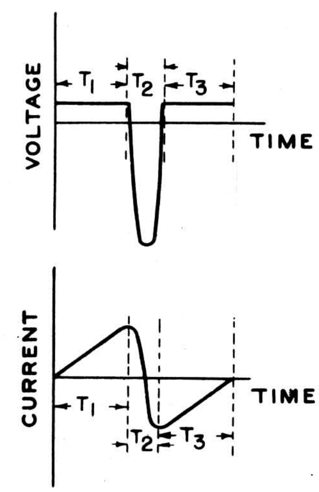
Actual circuit   Equivalent circuit

$$E = \frac{E_{T\,MAX}}{1 + \frac{\pi(1-\delta)}{2\delta}}$$

$$L = \left(\frac{K(1-\delta)E}{Df_h}\right)^2$$

$$I_{PP} = \frac{f_h D^2}{K^2 E(1-\delta)}$$

$$\sqrt{LC} = \frac{\delta}{\pi f_h}$$

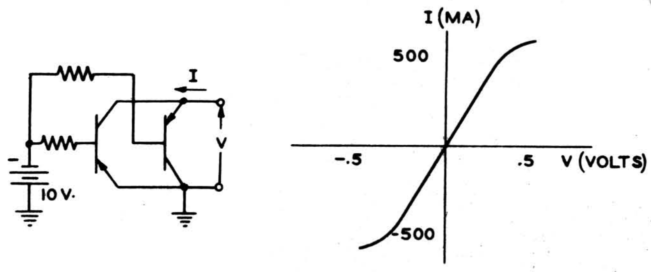


Design equations   Yoke waveforms

Fig. 12 - Horizontal deflection circuit and design equations.

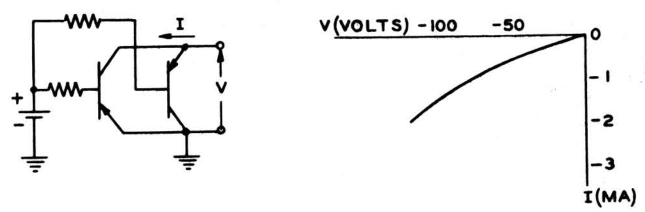
The use of transistors as the switching mechanism results in a simple and highly efficient circuit which closely approximates an ideal switch. In Fig. 13, two transistors with their emitters and collectors cross-connected are used in place of a single symmetrical transistor. Fig. 13 shows the output characteristics of the switching transistors in the "closed" and "open" conditions. The symmetry and low effective resistance of the "closed" condition (a) and the high effective resistance of the "open" condition (b) are apparent.

In order to control the output transistors, it is necessary that their bases be returned to a source of negative potential while they are conducting, and to a source of positive potential while they are cut off. This is accomplished with another form of switching circuit employing two transistors as shown in Fig. 14. The arrangement, which is essentially a single-pole double-throw switch, has been referred to as the "totem pole" circuit.



Circuit   VI characteristic

(a) "Closed" connection



Circuit   VI characteristic

(b) "Open" connection

Fig. 13 - Output characteristics of switching transistors.

During the forward trace of the beam, the first transistor, T_1, is in a high-conduction state because of the large negative bias applied through R_1, while T_2 is cut off. The bases of the output transistors are thus connected through T_1 to the negative $22\frac{1}{2}$-volt supply. When a positive pulse is applied to T_1 through C_1, T_1' is cut off and the resulting negative pulse across R_2 is coupled through C_2 to T_2 and causes T_2 to conduct heavily. For the duration of the positive pulse the bases of the output transistors are therefore connected through T_2 to the positive $22\frac{1}{2}$-volt supply.

The above discussion indicates that pulses occurring at line repetition rate and equal in width to the retrace time are necessary to operate the horizontal-deflection system. These pulses are obtained from an oscillator essentilly the same as is used for the vertical deflection except for the frequency determining components. Amplification of the pulses is provided by the direct-coupled complementary-symmetrical Class-B pulse amplifier shown in Fig. 15.

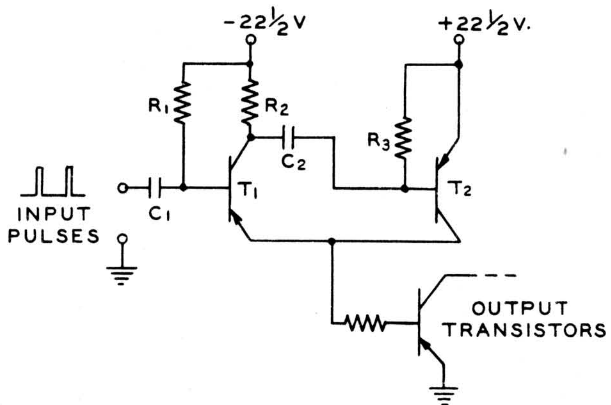


Fig. 14 – Totem pole circuit.

With no input signal, both transistors are nearly cut off, and the output terminal is connected through R_2 to the negative 22½-volt supply. A positive pulse at the input causes both transistors to conduct heavily and connects the output terminal to the positive 22½-volt supply through the p-n-p unit. With this circuit it is possible to obtain approximately 40-volt peak-to-peak output pulses from a peak-to-peak input of 0.5 volt.

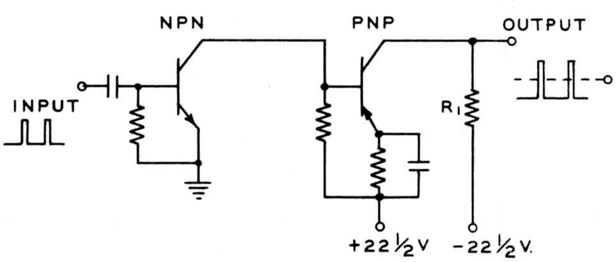


Fig. 15 – Direct-coupled pulse amplifier.

The preceding description implies that the elapsed time between the oscillator discharge and the opening of the switching transistors is negligible when compared to the time for one line retrace. If this were true, driven sync could be used. However, because of reactive effects associated with the input circuit of the switching transistors, there is appreciable time delay between the application of a positive pulse and the "opening" of the yoke circuit. Experimentally it was found that this delay is approximately 15 μsec which is about 5 μsec longer than the time allotted for horizontal retrace.

One effect of such a delay on the television picture is to place a black vertical bar at the right of the screen which corresponds to the horizontal blanking in the video signal. In addition, a portion of the picture appears immediately to the right of the black bar. It is apparent that an a-f-c system can compensate for the delay described above by re-phasing the horizontal oscillator. A simple and reliable transistor a-f-c system will be described in a later section.

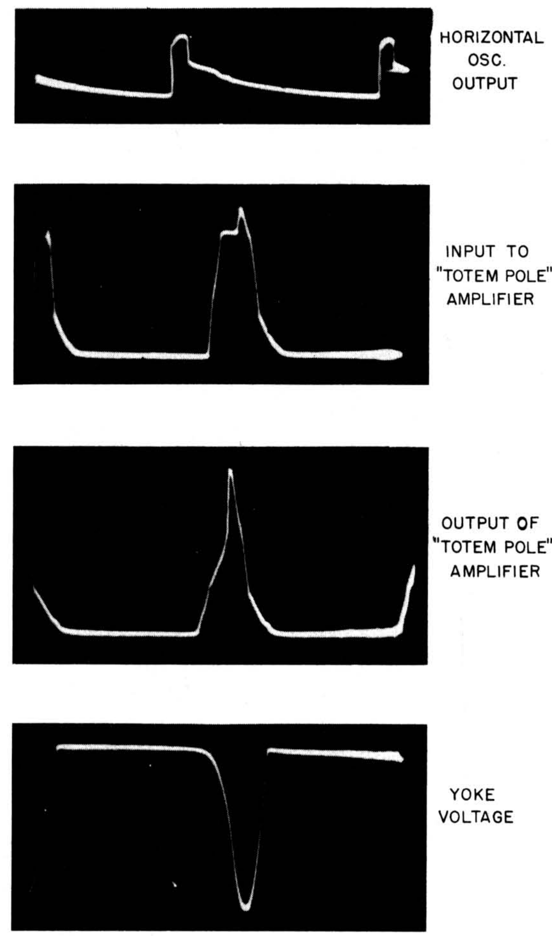


Fig. 16 – Waveforms in the horizontal deflection circuit.

Figs. 16 and 17 show photographs of the waveforms observed at several points in the horizontal deflection system. Of particular interest are those concerning the yoke voltage and current. The similarity of the photographed waveforms to those predicted by the elementary theory in Appendix B is evident.

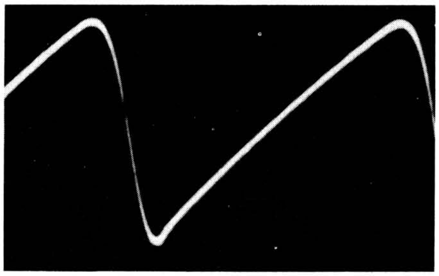


Fig. 17 - Horizontal yoke current waveform.

Sync Channel

A schematic of the synchronizing circuits of the receiver is shown in Fig. 18. The sync separator and amplifier consist of two TA-153 junction transistors. The first of these is connected grounded base. The emitter-base rectifier serves to separate the sync pulses which are coupled by the collector circuit to the following amplifier. After integration, the vertical pulses are amplified by a grounded emitter stage and are then used to synchronize the vertical oscillator.

The horizontal a-f-c system mentioned previously depends for its operation on the symmetrical properties of the phase comparator transistor. The retrace voltage pulse from the deflection yoke is integrated by a network consisting of R_1 and C_1. In the absence of a negative sync pulse on its base, the phase comparator functions simply as a high resistance and the integrated retrace pulse appears as a symmetrical sawtooth wave, its d-c component having been removed by C_2. There is therefore no d-c voltage on the base of the frequency control transistor.

The operation is unchanged if the horizontal sync pulse arrives coincident with the time of zero voltage during the sawtooth retrace. If the sync pulse arrives when the retrace voltage is positive, C_2 receives an incremental charge through the resulting low resistance of the phase comparator. During the time before the next sync pulse, this incremental charge drains off through R_4 and the frequency control transistor. A small negative bias is thus generated on the base of the frequency control transistor which lowers its effective resistance and causes the horizontal oscillator to fire sooner than on the previous cycle. The action continues until the sync pulse occurs simultaneously with the zero voltage point of the sawtooth retrace. The sequence of operation is reversed in the event the sync pulse originally arrives while the sawtooth retrace is negative.

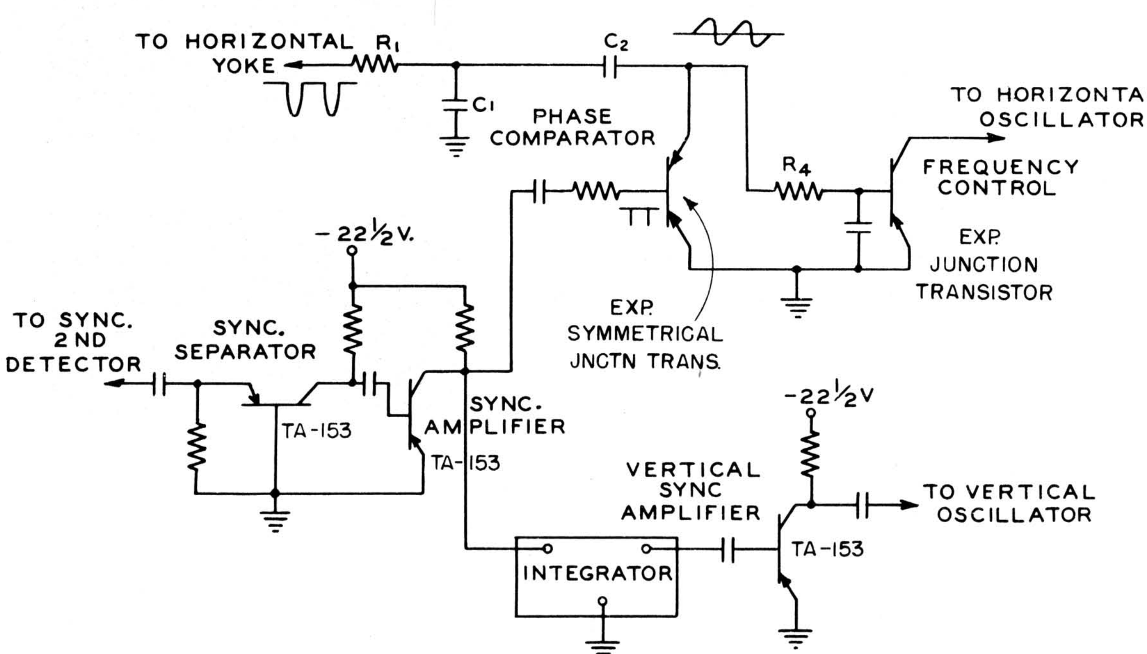


Fig. 18 - Sync channel and AFC circuits.

High-Voltage Supply

Because the flyback voltage of the horizontal deflection system is limited by transistor characteristics and since no transformer is used, it is not convenient to get the 2000-volt d.c. for the kinescope directly from the deflection system. For this reason a separate system shown in Fig. 19 was used. This is essentially a two-stage class-B amplifier driving a tuned transformer in the output. The negative flyback pulse is lightly coupled to the amplifier and causes the first transistor to conduct, thereby applying a conduction bias to the output stage. The output transistor, a power type, conducts heavily and supplies power to the tuned transformer at a horizontal frequency. The choke in the base circuit of the output transistor provides a low-impedance d-c path and insures that any leakage current in either transistor does not bias the output to conduction except when the system is pulsed. A half-wave selenium rectifier and filter provides the 2000-volt d.c. from the secondary of the tuned transformer.

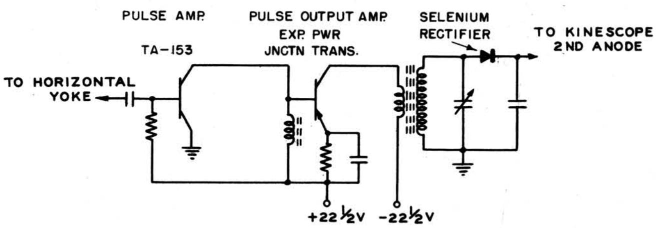


Fig. 19 - High voltage system.

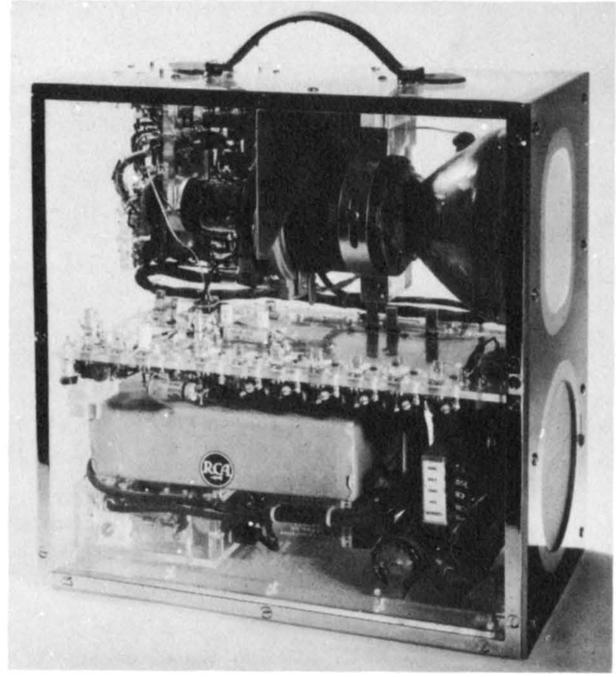


Fig. 20 - General layout of receiver.

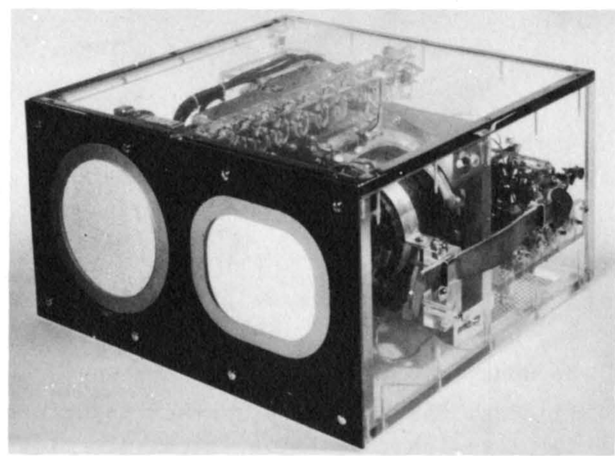


Fig. 21 - Front view of receiver.

Receiver Description

The receiver was built in a portable form with self-contained batteries in a clear plastic case. The total power consumption of the receiver is 13 watts. Of these 13 watts, 3.6 watts or more than 25 per cent, goes into the filament of the kinescope. The kinescope is the 5FP4 type and provides a 3 x 4-inch picture with a highlight brightness of approximately 10 foot-lamberts. The general layout of the receiver is shown in Fig. 20. The signal channel is built on the vertical plastic shelf in the center of the receiver. The deflection chassis is under the neck and the socket of the kinescope. The high-voltage supply is placed beyond the batteries to provide the least disturbance to the rest of the receiver. Fig. 21 shows the receiver in its normal viewing position. The total weight of the receiver with the batteries is 27 pounds.

Gerald B. Herzog

Robert D. Lohman

George C. Sziklai

Appendix A

With reference to Fig. 8:

$$V_b = -I_{co}R_3,$$

$$V_e = -\frac{VR_2}{R_1+R_2}\, e^{\frac{-t}{(R_1+R_2)}}$$

The condition for negligible emitter-collector conduction is:

$$|V_b| < |V_e|.$$

When this condition is no longer met, the discharge begins and is cumulative since:

$$I_b = I_{co} + I_E(\alpha-1).$$

$$\alpha > 1.$$

Appendix B

Horizontal Deflection System

The operation of the horizontal deflection will be described by assuming:

(1) that the yoke is a perfect inductance,

(2) that the transistor is a bi-directional switch with a constant resistance when closed and infinite resistance when open.

The circuit operation will be considered during three durations of time:

(1) T_1, during which the switch is closed

(2) T_2, during which the switch is open

(3) T_3, during which the switch is closed

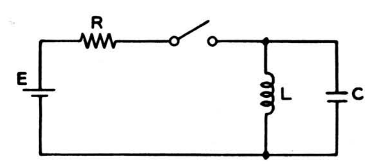
The relationships between these time durations are:

$$T_1 = T_3, \quad (1)$$

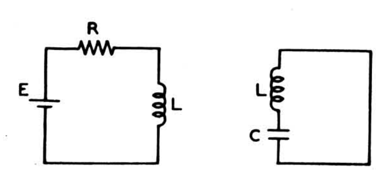
$$\frac{T_2}{T_1+T_2+T_3} = \delta, \quad (2)$$

$$T_1+T_2+T_3 = 1/f_h \quad (3)$$

where δ is the ratio of the retrace time to the time for one complete cycle and f_h is the line repetition rate. The simplified circuit is shown in Fig. 22a.



(a) Simplified equivalent circuit.



(b) Circuit during T_1 and T_3

(c) Circuit during T_2

Fig. 22 - Circuits of Appendix B analysis.

The circuit may be further simplified as shown in Fig. 22b and c for each of the three time intervals if the following additional assumptions are made:

$$RC \ll T_1; \qquad \frac{R}{L} T_1 \ll 1 \tag{4}$$

The operation during the interval T_1 is as follows:

$$I(t)R + L\frac{dI(t)}{dt} = E, \tag{5}$$

$$I(0) = 0 \tag{6}$$

The solution is:

$$I(t) = \frac{E}{R}\left(1 - e^{\frac{-tR}{L}}\right), \tag{7}$$

$$I(t) \approx \frac{E}{L} t, \text{ since } \frac{R}{L} T_1 \ll 1 \tag{8}$$

The operation during T_2 while the switch is open is as follows:

$$L\frac{dI(t)}{dt} + \frac{1}{C}\int I(t)dt = 0, \tag{9}$$

$$I(0) = \frac{E}{L} T_1. \tag{10}$$

The solution is:

$$I(t) = \frac{E}{L} T_1 \cos t/\sqrt{LC}. \tag{11}$$

where time is measured from the instant of opening the switch. If the switch remains open for a time such that:

$$\frac{t}{\sqrt{LC}} = \pi = \frac{T_2}{\sqrt{LC}}, \tag{12}$$

then,

$$T_2 = \pi\sqrt{LC}. \tag{13}$$

Thus, at the end of T_2 the current in the yoke has reversed and the resonant circuit has gone through one-half cycle of oscillation.

The operation during T_3 is as follows:

$$RI(t) + L\frac{dI(t)}{dt} = E, \tag{14}$$

$$I(0) = -\frac{E}{L} T_1. \tag{15}$$

The solution in this case is:

$$I(t) \approx \frac{E}{L} t - \frac{E}{L} T_1 + \frac{RE}{L^2} T_1 t, \tag{16}$$

$$I(t) = \frac{E}{L} t \left(1 + \frac{T_1}{L/R}\right) - \frac{E}{L} T_1,$$

$$I(t) \approx \frac{E}{L} t - \frac{E}{L} T_1. \tag{17}$$

since the assumption that $RT_1/L \ll 1$ has already been made. The current during T_3 is therefore a linear time function minus a constant current. At the end of T_3 the linear term equals the constant term and the current is zero. The cycle then repeats.

It is desirable to eliminate the three intervals of time T_1, T_2 and T_3 from the equations since they can be expressed in terms of L, C, δ, and f_h. This may be done as follows: From Eqs. (13), (2), and (3):

$$T_2 = \pi\sqrt{LC}, \tag{18}$$

$$T_1 = \frac{T_2(1-\delta)}{2\delta} = \frac{\pi\sqrt{LC}(1-\delta)}{2\delta} = T_3, \tag{19}$$

$$\sqrt{LC} = \frac{\delta}{\pi f_h} \tag{20}$$

The idealized waveforms for the complete cycle are shown in Fig. 12.

In designing the horizontal deflection system it is necessary to derive several relationships which connect the magnitude of the deflection to the equations determined in the previous discussion. The design is limited by the voltage rating of the switching transistors, the particular yoke and kinescope construction used, and the anode voltage chosen for the kinescope.

Let:

- K = a measurable constant depending on yoke construction and anode voltage,
- D = deflection width in inches,
- δ = ratio of retrace time to the time for one complete cycle,
- L = inductance of yoke in henries,
- f_h = line repetition rate in cycles/sec.,
- E = battery voltage in volts.

If I_{pp} = peak-to-peak deflection current in amperes, it can be shown that:

$$I_{pp} = \frac{D}{K\sqrt{L}} = \frac{E}{L}(T_1+T_3). \qquad (21)$$

From Eqs. (1) and (19):

$$T_1+T_3 = 2T_1 = \frac{\pi\sqrt{LC}(1-\delta)}{\delta}. \qquad (22)$$

From Eq. (20):

$$\sqrt{LC} = \frac{\delta}{\pi f_h}. \qquad (20)$$

Therefore:

$$L = \left[\frac{K(1-\delta)E}{Df_h}\right]^2, \qquad (23)$$

$$I_{pp} = \frac{f_h D^2}{K^2 E(1-\delta)}. \qquad (24)$$

For a given deflection width, repetition rate, yoke construction, kinescope construction, and anode voltage, it is seen that both L and I_{pp} are dependent only on E and δ. With the transistors used, E is uniquely determined by δ and the maximum allowable voltage across the transistors.

The maximum voltage across the yoke inductance may be found from Eq. (11).

$$I_L = \frac{E}{L}T_1 \cos t/\sqrt{LC}, \qquad (11)$$

$$E_L = L\frac{dI_L}{dt} = -\frac{E\pi(1-\delta)}{2\delta} - \sin T/\sqrt{LC} \qquad (25)$$

This expression is a maximum when:

$$\sin t/LC = 1 .$$

Therefore,

$$\hat{E}_L = \frac{-\pi(1-\delta)E}{2\delta}. \qquad (26)$$

The maximum voltage across the transistors, E_T, is:

$$\hat{E}_T = \hat{E}_L + E. \qquad (27)$$

where the signs must be chosen so the voltages add:

$$\hat{E}_T = -E\ 1 + \frac{\pi(1-\delta)}{2\delta} \qquad (28)$$