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LB-875

TRANSISTOR TRIGGER CIRCUITS

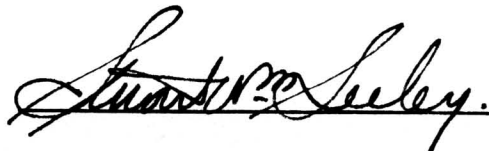
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LB-875**Transistor Trigger Circuits**

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ApprovedA handwritten signature in cursive script, appearing to read "Stuart M. Seley", is written over a horizontal line.

Transistor Trigger Circuits

Introduction

This bulletin concerns trigger and pulse circuits for transistors having emitter-to-collector current gain (such as point-contact units). The circuits are designed to permit reliable operation with transistors which are not completely uniform; and they also allow reasonable variation of circuit parameters or bias voltages. Quantitative analysis is made possible by use of simplified circuit theory which divides the non-linear characteristic of a transistor and its associated feedback and external resistances into quasi-linear regions. By this analysis, one can predict both the type of operation, i.e., monostable, bistable and astable (oscillatory), and the amplitude and wave form of the output.

A basic monostable circuit consists of a single transistor with a resistance in the base lead to provide feedback and a capacitance or, preferably, a transmission line in the emitter lead. This circuit can be used to regenerate periodic or non-periodic pulses, providing a standardized output pulse shape, or to generate single pulses when initiated; it is possible to provide very intense short pulses (up to one ampere) even with transistors of low power-handling ability. The output pulses may be arbitrarily delayed with respect to the input, and amplitude discrimination against noise or spurious signals is also possible.

Bistable circuits also use a single transistor with external resistances. It is shown that lack of reliability of previously used bistable single-transistor circuits can be overcome by proper arrangement of circuit parameters and bias supplies and, in some cases, by use of a non-linear resistance (crystal diode) as the emitter load. Laboratory experience indicates that such single-transistor circuits can be made highly reliable and will allow interchangeability of transistors and reasonable variations in power supplies, etc. In these respects, they have been made superior even to earlier twin-transistor bistable circuits in which reliability had been emphasized. A small, light-weight decade counter was designed with these single-transistor bistable circuits; it uses less than 2 watts of power in contrast to a well-designed electron-tube counter which needs 60 watts, uses twice as many amplifier elements and requires considerably more weight and space.

General Discussion

Circuits employing a single point-contact transistor (or other transistor with emitter-to-collector current gain greater than unity) together with passive circuit elements may be made to have two distinct stable states separated by an unstable negative-resistance region. The circuit can be made to trigger from one stable state to the other in a very short time by the application of an input pulse. The trigger action suggests the use of this type of transistor in circuits where the output is to be controlled by the presence of an input pulse and where the faithful reproduction of the input signal is not required.

Earlier investigations in this field resulted in the development of a number of novel circuits. Laboratory experience, however, revealed that the operation of most transistor circuits was so critical as to limit their applications in systems where reliability was

of primary importance. Transistors presently available match much more closely in their characteristics than early units but are still not completely uniform; temperature changes also affect their characteristics. In this bulletin, special consideration has been given in these respects to the design of practical and novel transistor circuits so as to achieve reliability which has not been previously attained.

Part I of this bulletin presents a simplified analysis of transistor trigger circuits which will assist in the understanding of their operation and which will serve as a guide for the design of practical circuits. Part II includes a number of practical pulse-handling circuits, the satisfactory operation of which is not impaired by reasonable variations of circuit parameters, bias voltages, transistor characteristics, and ambient temperature.

Part I. A Simplified Analysis of Transistor Trigger Circuits

Basic Trigger Circuit

Some simple circuits employing a single transistor may perform trigger action by virtue of the current-amplification within the transistor and the positive feedback afforded by base resistance (both internal and external). A rigorous analysis is difficult because of the high degree of nonlinearity involved. However, certain approximations may be made to simplify the analysis without loss of effectiveness.* The following simplified analysis, derived from experimental results, may serve effectively to explain and describe the operation of these circuits and to guide in their design.

A basic trigger circuit is shown in Fig. 1.^{1, 3} The operation of this circuit may be monostable, bistable, or astable (oscillatory) depending on the nature of the emitter load. For practical purposes the behavior of the circuit is adequately described by the two characteristics* shown in Fig. 2: (a) the Emitter Input Characteristic (V_e -- i_e curve),

and (b) the Current Transfer Characteristic (i_c -- i_e curve). The V_e -- i_e curve, together with the emitter load line, dictates the mode of operation of the circuit, while the i_c -- i_e curve determines the form of the output signal.

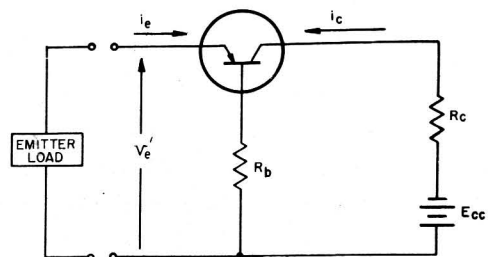


Fig. 1 - Basic trigger circuit.

Considering i_e as the independent variable, each curve exhibits three distinct regions, namely, a low-conduction "cutoff" region, a negative resistance "transition" region, and a high-conduction "saturation" region. The curves in each region do not deviate appreciably from straight lines, except near the boundaries.

*These characteristics are of the complete circuit including the transistor.

This property indicates that the circuit may be represented by three equivalent circuits, one for each region.

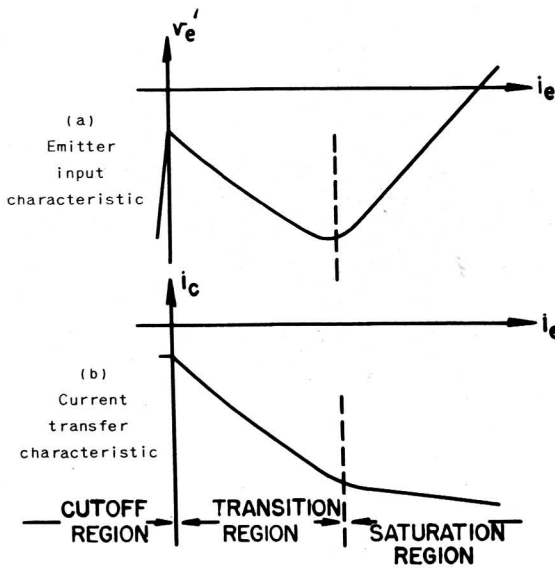


Fig. 2 - Trigger circuit characteristics.

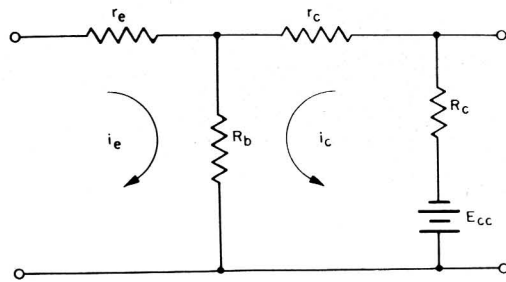


Fig. 3 - Equivalent circuit - cutoff region.

Following conventional notation, the transistor may be represented by its internal resistances r_e , r_b and r_c , and a current source αi_e . The value of r_b is usually small compared with external base resistance R_b . In the cutoff region, where $i_e < 0$, the transistor is characterised by its high r_e and zero current-amplification. The equivalent circuit for this region is shown in Fig. 3. The Emitter Input characteristic for the cutoff region is represented by the equation:

$$V_e' \approx i_e r_e - \frac{R_b}{R_b + R_c + r_c} E_{cc} \quad (1)$$

whose slope and intersection are respectively:

$$\frac{\partial V_e'}{\partial i_e} \approx r_e \quad (2)$$

$$V_e' = - \frac{R_b}{R_b + R_c + r_c} E_{cc}, \text{ at } i_e = 0$$

The Current Transfer Characteristics for the cutoff region is represented by:

$$i_c = - \frac{R_b}{R_b + R_c + r_c} i_e - \frac{E_{cc}}{R_b R_c r_c} \quad (3)$$

or

$$\frac{\partial i_c}{\partial i_e} = - \frac{R_b}{R_b + R_c + r_c} \quad (4)$$

$$i_c = - \frac{E_{cc}}{R_b + R_c + r_c}, \text{ at } i_e = 0$$

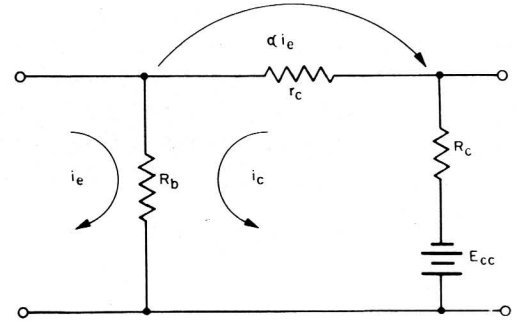


Fig. 4 - Equivalent circuit - transition region.

In the transition region, where $r_e \ll R_b$ and $\alpha > 1$, the equivalent circuit is shown in Fig. 4. The Emitter Input Characteristic for the transition region is:

$$V_e' = \frac{R_b [R_c + r_c (1 - \alpha)]}{R_b + R_c + r_c} i_e - \frac{R_b}{R_b + R_c + r_c} E_{cc} \quad (5)$$

or

$$\frac{\partial V_e'}{\partial i_e} = \frac{R_b [R_c + r_c (1 - \alpha)]}{R_b + R_c + r_c}$$

$$V_e' = - \frac{R_b}{R_b + R_c + r_c} E_{cc}, \text{ at } i_e = 0 \quad (6)$$

The Current Transfer Characteristic for the transition region is:

$$i_c = - \frac{R_b + \alpha r_c}{R_b + R_c + r_c} i_e - \frac{E_{cc}}{R_b + R_c + r_c} \quad (7)$$

or

$$\frac{\partial i_c}{\partial i_e} = - \frac{R_b + \alpha r_c}{R_b + R_c + r_c}$$

$$i_c = - \frac{E_{cc}}{R_b + R_c + r_c}, \text{ at } i_e = 0 \quad (8)$$

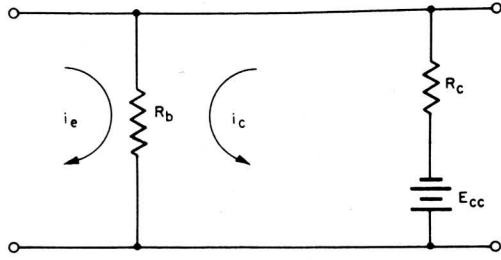


Fig. 5 - Equivalent circuit - saturation region.

In the saturation region the transistor behaves approximately like a conductor, suggesting the approximate equivalent circuit shown in Fig. 5. The Emitter Input Characteristic for the saturation region is approximately,

$$V'_e = \frac{R_b R_c}{R_b + R_c} i_e - \frac{R_b}{R_b + R_c} E_{cc} \quad (9)$$

or

$$\frac{\partial V'_e}{\partial i_e} = \frac{R_b R_c}{R_b + R_c}$$

$$i_e = \frac{E_{cc}}{R_c}, \text{ at } V'_e = 0 \quad (10)$$

The Current Transfer Characteristic for the saturation region is approximately,

$$i_c = - \frac{R_b}{R_b + R_c} i_e - \frac{E_{cc}}{R_b + R_c} \quad (11)$$

$$\frac{\partial i_c}{\partial i_e} = - \frac{R_b}{R_b + R_c}$$

(12)

$$i_c = - \frac{E_{cc}}{R_b + R_c}, \text{ at } i_e = 0$$

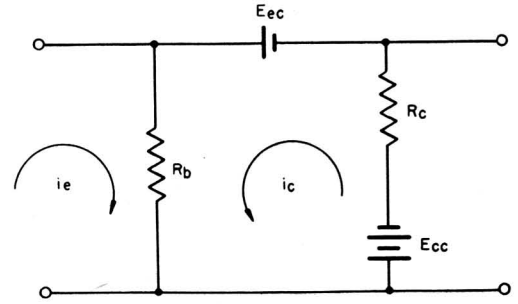


Fig. 6 - Modified equivalent circuit - saturation region.

The assumption that the transistor acts like a perfect conductor in the saturation region is an approximation suited for a first approach. Actually the values of R_e , r_b , and r_c , at high conduction are small but not negligible, and they do not remain constant with changes of i_e . Laboratory investigation, however, reveals the existence of a small voltage between emitter and collector, which is substantially constant over the entire saturation region. For a better approximation, therefore, the equivalent circuit for the saturation region is modified as shown in Fig. 6. The more exact Emitter Input Characteristic for the saturation region is

$$V'_e = \frac{R_b R_c}{R_b + R_c} i_e - \frac{R_b}{R_b + R_c} (E_{cc} - E_{ec}) \quad (9a)$$

or

$$\frac{\partial V'_e}{\partial i_e} = \frac{R_b R_c}{R_b + R_c}$$

$$i_e = \frac{E_{cc} - E_{ec}}{R_c}, \text{ at } V'_e = 0 \quad (10a)$$

The more exact Current Transfer Characteristic for the saturation region is:

$$i_c = - \frac{R_b}{R_b + R_c} i_e - \frac{E_{cc} - E_{ec}}{R_b + R_c} \quad (11a)$$

or

$$\frac{\partial i_c}{\partial i_e} = - \frac{R_b}{R_b + R_c}$$

$$i_c = - \frac{E_{cc} - E_{ec}}{R_b + R_c}, \text{ at } i_e = 0 \quad (12a)$$

Based upon this simplified analysis, using Eqs. (1) to (12), the calculated characteristics and experimental results are plotted for a typical circuit, as shown in Figs. 7a and 7b. Close agreement between the experimental and analytical curves is observed both in the cutoff region and in the saturation region.

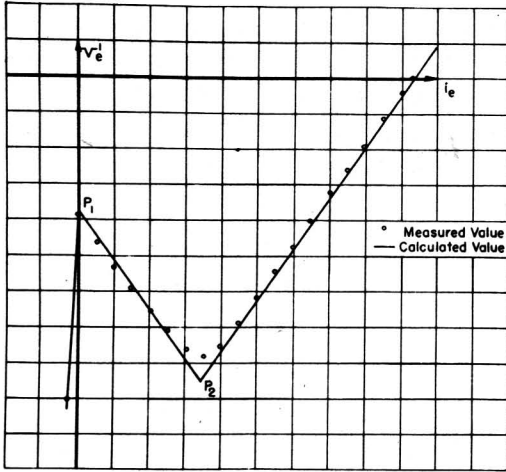


Fig. 7(a) - Emitter input characteristic.

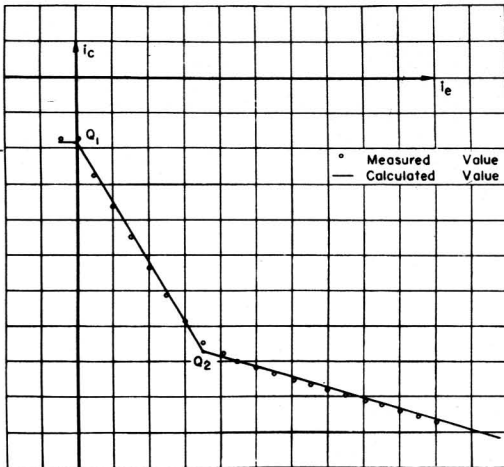


Fig. 7(b) - Current transfer characteristic.

Agreement is not expected, of course, where the observed curve departs from linearity. In the transition region the curves depart considerably from a straight line. This is due to the fact that the values α and r_c do not remain constant with change of i_e as assumed in the analysis. However, in most pulse handling circuits the exact shape of the curve in the transition region is not important as long as the turn-over points P_1 , P_2 , Q_1 and Q_2 are well defined. From Eqs. (1) to (12) the calculated coordinates of the turn-over points are:

$$P_1: \quad i_e = 0, \quad V_e' = -\frac{R_b}{R_b + R_c + r_c} E_{cc} \quad (13)$$

$$Q_1: \quad i_e = 0, \quad i_c = -\frac{E_{cc}}{R_b + R_c + r_c} \quad (14)$$

$$P_2: \quad i_e = \frac{E_{cc}}{\alpha(R_b + R_c) - R_b}, \quad V_e' = \frac{R_b(1-\alpha)E_{cc}}{\alpha(R_b + R_c) - R_b} \quad (15)$$

$$Q_2: \quad i_e = \frac{E_{cc}}{\alpha(R_b + R_c) - R_b}, \quad i_c = \frac{-\alpha E_{cc}}{\alpha(R_b + R_c) - R_b} \quad (16)$$

The points, P_1 and Q_1 , where the circuit is triggered from low to high conduction, depend on the value of r_c which, unfortunately, is affected considerably by temperature and which also varies from unit to unit. The points, P_2 and Q_2 , where the circuit is triggered from high to low conducting, depend mainly on α which decreases with increasing i_e . The calculated coordinates of P_2 and Q_2 , based on the assumption that α remains constant, depart considerably from the measured values in V_e' but check fairly well in i_e and i_c . This is a favorable situation as far as the design of practical circuits is concerned.

The analysis of this type of circuit is not limited to the emitter characteristic alone; rather it is subject to a like development of the base and collector characteristics. In general, the approach is valid at any branch in the circuit where negative resistance is exhibited. The emitter input approach offers some advantages in simplicity, however.

Monostable Circuits

A basic monostable circuit is shown in Fig. 8 together with its emitter input characteristic and its current transfer characteristic. These two curves may be referred to jointly in the following discussion. The negative resistance region of the $V_e'--i_e$ curve begins slightly to the right of the $V_e'--$ axis. In the quiescent state the condenser, C , constitutes an open-circuit in the emitter loop. The quiescent operation point is at the point M_1 , which is the intersection between the open-circuit load line (the $V_e'--$ axis) and the $V_e'--i_e$ curve. When a trigger source sends into the emitter a positive current greater than I_1 , the

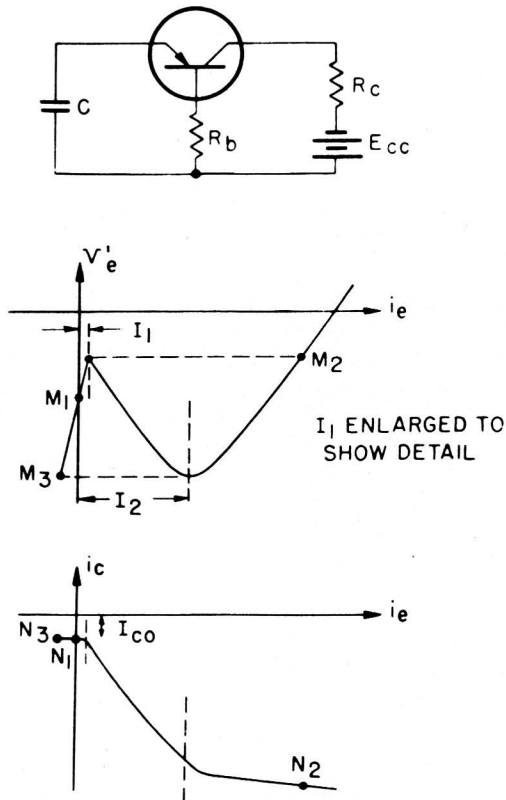


Fig. 8 - Basic monostable circuit.

circuit passes into its unstable negative resistance region. By virtue of the current-amplification within the transistor and the positive feedback action afforded by the base resistance the emitter and collector currents increase rapidly, which results in the sudden jump of i_e to the point M_2 in the saturation region. In the process of charging the condenser C in the emitter loop i_e diminished until its value is less than I_2 . At this point the circuit re-enters the unstable region and quickly jumps back to point M_3 in the low conduction stable state. Eventually, as a consequence of the discharge of capacitor C , the initial quiescent operating point M_1 is attained.

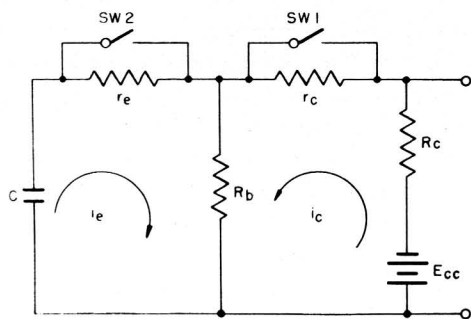


Fig. 9 - Equivalent circuit of trigger action.

Referring now to the equivalent circuit of the two states, Figs. 3 and 5, the operation of the circuit is seen to resemble a simple switching problem as shown in Fig. 9. The switches SW_1 and SW_2 are open-circuited in the quiescent state. At $t = 0$, corresponding to application of the trigger pulse, both switches are closed. It is readily shown by Laplace-transformation analysis that the emitter and collector currents as functions of time may be expressed by:

$$i_e = \frac{E_o}{R_c} e^{-\frac{1}{R_{//}C} t} ; 0 < t < T \quad (17)$$

$$i_c = -\frac{R_b E_o}{R_c (R_b + R_c)} e^{-\frac{1}{R_{//}C} t} - \frac{E_{cc}}{R_b + R_c} ; 0 < t < T$$

where

$$E_o \equiv \frac{r_c}{R_b + R_c + r_c} E_{cc} \quad (18)$$

$$R_{//} \equiv \frac{R_b R_c}{R_b + R_c}$$

The analysis reveals that i_e jumps from zero E_o/R_c on application of the trigger pulse, and then decrease exponentially with times at a rate determined by the time constant $CR_{//}$. When i_e falls below the value I_2 , the circuit re-enters the negative resistance region and triggers back to the low conduction state. The value of I_2 , calculated by equating Eq. (5) and Eq. (9) is:

$$I_2 = \frac{E_{cc}}{\alpha (R_b + R_c) - R_b} \quad (19)$$

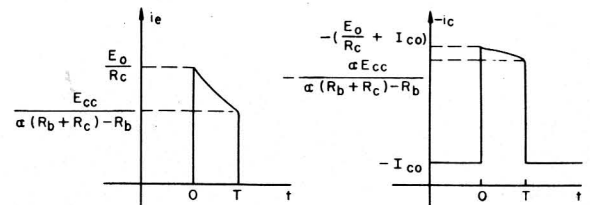


Fig. 10 - Emitter and collector current wave-forms.

This second trigger action is equivalent to opening switches SW_1 and SW_2 at $i_e = I_2$. The collector current varies in a like manner (Fig. 10). The amplitude of the output voltage pulse is approximately E_o and its width (which

is the same as the width of the emitter current pulse) is:

$$T = R_{//} C \ln \frac{r_c [\alpha (R_b + R_c) - R_b]}{(R_b + R_c + r_c) R_c} \quad (20)$$

Note that the generated pulse width is independent of E_{cc} . Eqs. (17) and (18), based on the saturation state equivalent circuit, are valid only in the interval $0 < t < T$. In other words:

$$i_e = \frac{E_o}{R_c} e^{-\frac{1}{R_{//} C} t}, \quad \text{for } 0 < t < T \quad (21)$$

$$= 0, \quad \text{for } t < 0, t > T$$

$$i_c = \frac{-E_o R_b}{R_c (R_b + R_c)} e^{-\frac{1}{R_{//} C} t} - \frac{E_{cc}}{R_b + R_c}, \quad \text{for } 0 < t < T \quad (22)$$

$$= \frac{-E_{cc}}{R_b + R_c + r_c}, \quad \text{for } t < 0, t > T$$

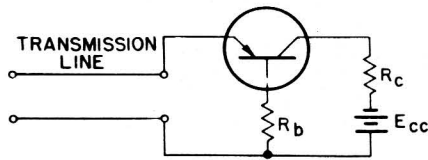


Fig. 11 - Transmission line controlled monostable circuit.

The output pulse departs from the ideal flat-topped pulse according to the exponential term of Eq. (18). This departure is more pronounced when R_c is small, which is the case when a high current pulse is desired. The output pulse width is a function of α and r_c (Eq. 20) which may vary from unit to unit and which may also be temperature dependent. For precision applications it is desirable to have a circuit whose output waveform is controlled by circuit parameters alone. One such circuit employing a transmission line is shown in Fig. 11.⁹ For the following analysis let the emitter load be an open-circuited loss-less line with a surge impedance $R_0 = \frac{R_b R_c}{R_b + R_c}$ and of such length that the delay time is $T/2$. Treating the problem in the same manner as was described in connection with its archetype, the emitter and

collector currents as functions of time may be expressed as:

$$i_e = \frac{E_o}{2R_c} [U(t) - U(t-T)] \quad (23)$$

$$i_c = \frac{E_o}{2R_c} [U(t) - U(t-T)] - \frac{E_o}{2(R_b + R_c)} [U(t) - U(t-T)] - I_{co}$$

where

$$I_{co} \equiv \frac{E_{cc}}{R_b + R_c + r_c} \quad (24)$$

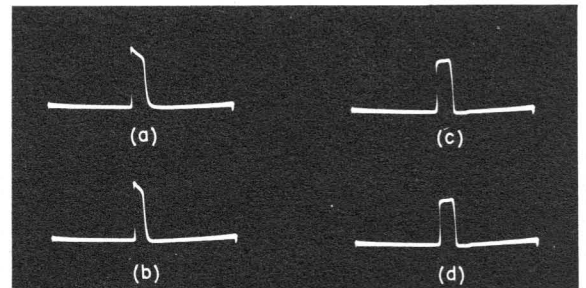
These expressions, based on the equivalent circuit for the saturation region, are valid only when $i_e > I_2$. Since i_e drops from $\frac{E_o}{2R_c}$ to 0 at $t = T$, the expressions are valid only during the time interval $0 < t < T$. The general expressions i_e and i_c are:

$$i_e = \frac{E_o}{2R_c}, \quad \text{for } 0 < t < T$$

$$= 0, \quad \text{for } t < 0, t > T \quad (25)$$

$$i_c = -\frac{R_b E_o}{2R_c (R_b + R_c)} - \frac{E_{cc}}{R_b + R_c}, \quad \text{for } 0 < t < T \quad (26)$$

$$= I_{co}, \quad \text{for } t < 0, t > T$$



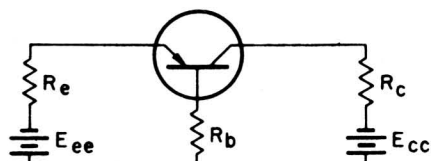
- (a) Condenser controlled, transistor 1.
- (b) Condenser controlled, transistor 2.
- (c) Transmission line controlled, transistor 1.
- (d) Transmission line controlled, transistor 2.

Fig. 12 - Output waveforms of two monostable circuits.

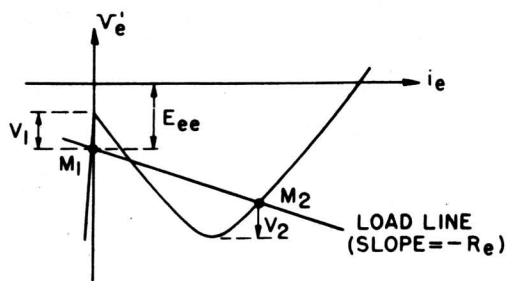
From Eqs. (25) and (26) it is evident that the values of i_e and i_c are constant (depending on circuit parameters only) during the time interval $0 < t < T$. The width of the current pulse is controlled solely by the transmission line, which may be precisely designed and built. The advantage of employing a transmission line instead of a condenser as the emitter load of the basic monostable circuit is illustrated in a typical case as shown in Fig. 12.

Bistable Circuit

A basic bistable circuit^{4, 8} and its operating characteristics are shown in Fig. 13a and 13b. The emitter load consists of a resistance R_e and a bias voltage E_{ee} .



(a) Circuit arrangement.

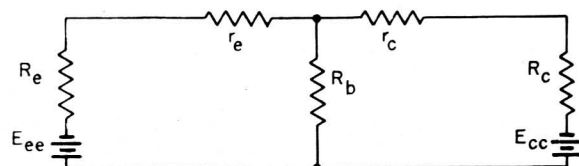


(b) Emitter input characteristic.

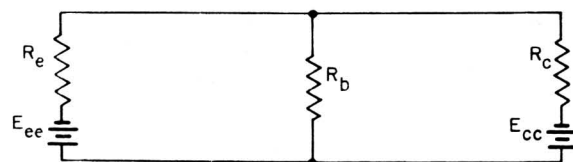
Fig. 13 - Basic bistable circuit.

A fundamental requirement for bistable operation is that the emitter load line intersect the v'_e-i_e curve once in each region. The circuit may stay at the low-conduction operation point M_1 (the OFF state) or at the high-conduction operation point M_2 (the ON state). The equivalent circuits of the two states are shown in Fig. 14, and the emitter and collector currents in either state may be computed accordingly. Referring to Fig. 13, a positive voltage V_1 may trigger the circuit from its OFF state to its ON state, and a negative voltage V_2 may perform the reverse operation. The

values of V_1 and V_2 may be made small to favor trigger sensitivity, or they may be made fairly large to insure reliable operation in the presence of noise, temperature change, and individual difference between transistor units.



(a) OFF STATE



(b) ON STATE

Fig. 14 - Equivalent circuits of the bistable circuit.

In practice, the chosen values of R_e and E_{ee} are a compromise between sensitivity and stability. However, the ultimate limits of the two parameters are:

$$R_e < \left| \frac{R_b [R_c + r_c (1-\alpha)]}{R_b + R_c + r_c} \right|$$

$$\left| \frac{R_b}{R_b + R_c + r_c} E_{cc} \right| < |E_{ee}| < \left| \frac{R_b (1-\alpha)}{\alpha (R_b + R_c) - R_b} E_{cc} \right|$$

as is evident from Fig. 13b, and Eqs. (5), (13) and (15).

Astable Operation

A simple transistor circuit may perform astable operation if the d-c operation point lies in the unstable negative resistance region and some reactive element is incorporated in the circuit.^{1, 7, 8} In Fig. 15a, the emitter is current-biased through a high resistance R_e so that the d-c operation point is some point P in the negative resistance region. A condenser C may supply the required reactance for non-sinusoidal RC oscillation, and a series resonant circuit may be employed for sinusoidal wave oscillation. A similar situation exists in the

collector circuit (Fig. 15b). In the base circuit, (Fig. 15c), the circuit may be voltage-biased through zero resistance in the base to obtain the proper d-c operation point. An inductance or a parallel resonant circuit may be employed to perform the astable operation.

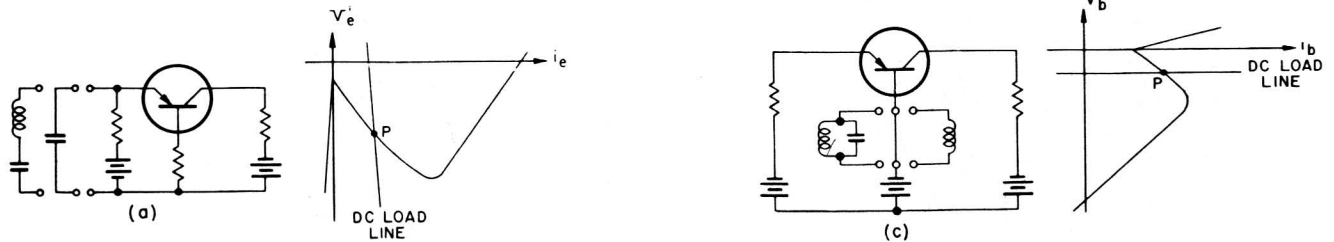


Fig. 15 - Basic astable circuits.

Part II. Some Practical Transistor Pulse-Handling Circuits

Monostable Circuits

The basic monostable circuit described in Part I, provides a regenerative amplifier with unique application possibilities. A practical pulse standardization circuit is shown in Fig. 16a. A negative-going trigger pulse, applied at the base of the transistor, initiates the trigger action. Because of the presence of the crystal diode CD_2 the input source is isolated from the transistor circuit except for the short duration when the initiation of trigger action takes place. The output pulse amplitude and width are practically independent of input pulse width and amplitude (Fig. 17).

It is observed that after the circuit triggers from its saturation state to its cutoff state the condenser C starts to discharge through the internal emitter resistance r_e which is high in the quiescent state. This discharge time limits the upper repetition frequency at which the circuit can be operated. To reduce the discharge time, a second diode CD_1 (Fig. 16a) is placed between emitter and collector to provide a low impedance path for the discharge of the condenser. The effective-

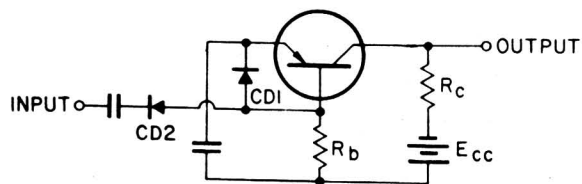
ness of this measure is illustrated by the waveform photography of Fig. 18.

Typical performance of the pulse standardization circuit is summarized in Table I and some output voltage waveforms are shown in Fig. 19.

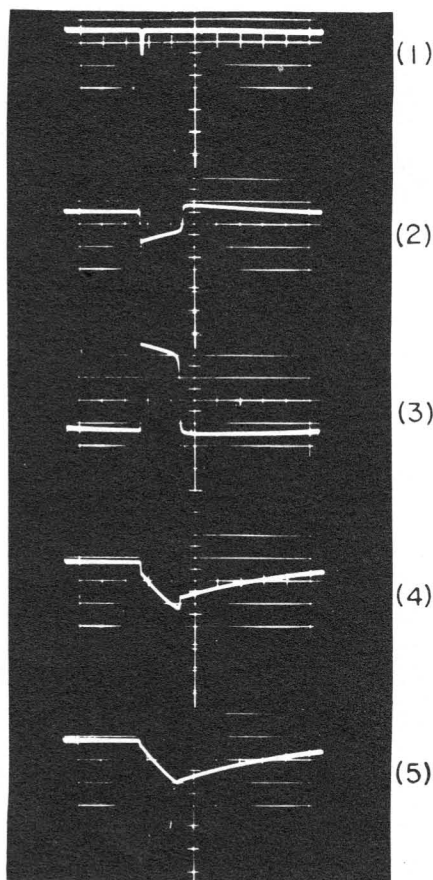
Table I

Performance of Pulse Standardization Circuit			
	$C = 470 \mu\text{f}$	$C = 2200 \mu\text{f}$	$C = 0.01 \mu\text{f}$
Output Pulse Amplitude (volts)	40	40	40
Output Pulse Width (μs)	0.25	1.1	5
Output Pulse Rise Time (μs)	0.02	0.02	0.02
Output Pulse Fall Time (μs)	0.1	0.1	0.1
Max. Voltage Gain	80	80	80

As the width of the output pulse may be readily prescribed by choosing proper circuit parameters, it is feasible to utilize the trailing edge of the output pulse to give a delayed pulse. As shown in Fig. 20a, a peaking coil and a damping diode are arranged in the collector circuit to generate a sharp pulse when the collector current jumps back from its saturation value. Some typical waveforms are shown in Fig. 20b.



(a) Circuit arrangement.



(b) Waveforms.

- (1) Input pulse.
- (2) Emitter current.
- (3) Collector current.
- (4) Base voltage.
- (5) Emitter voltage.

Fig. 16 - Pulse standardization circuit.

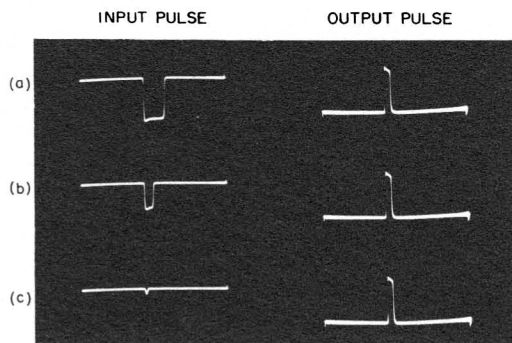
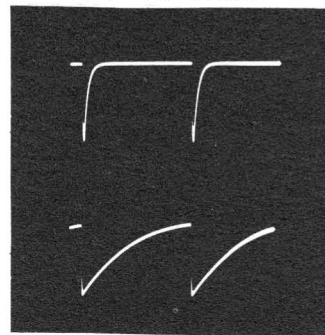


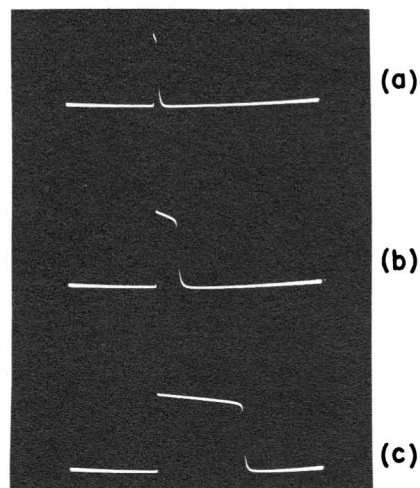
Fig. 17 - Input and output waveforms of pulse standardization circuit.

(a) With diode.



(b) Without diode.

Fig. 18 - Circuit recovery time.

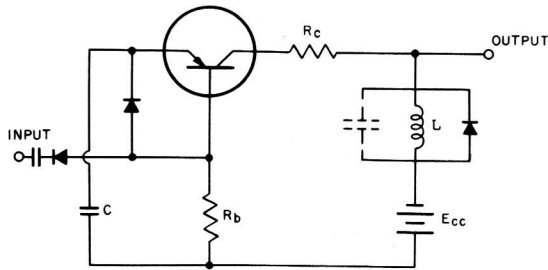


- (a) $C = 470 \mu\text{f}$
- (b) $C = 2200 \mu\text{f}$
- (c) $C = 0.01 \mu\text{f}$

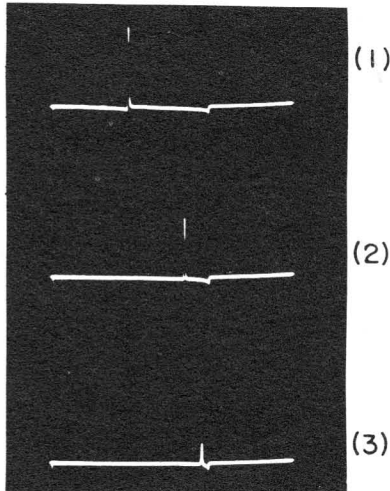
Fig. 19 - Output waveforms of pulse standardization circuit.

For those applications where a single, manually-initiated pulse is desired, the circuit of Fig. 21 will be of particular interest. In switching condenser C into the emitter circuit the charging current of the condenser triggers the circuit, generating a single output pulse.

When the external collector resistance R_c is reduced to a very small value, the monostable circuit is capable of delivering high-current pulses of short duration. This is evident from an inspection of the saturation region equivalent circuit and its analysis. Output pulses of current as high as one ampere (10 volts across a 10-ohm resistance) were observed in such a circuit using ordinary point-contact transistors. The extremely low output impedance of this circuit is of great value in driving low



(a) Circuit arrangement.



(b) Output waveforms.

- (1) $C = 470 \mu\text{f}$
- (2) $C = 2200 \mu\text{f}$
- (3) $C = 0.01 \mu\text{f}$

Fig. 20 - Pulse delay circuit.

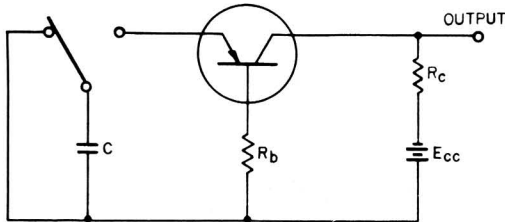


Fig. 21 - Single-shot pulse generator.

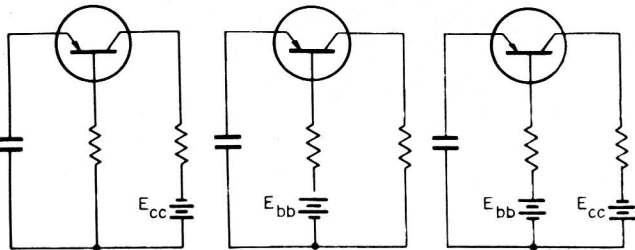


Fig. 22 - Location of power supply voltage.

impedance networks or in operating in a system where distributed capacitance is an important consideration in design.

The power supply voltage E_{cc} in the basic monostable circuit may be located in the collector and base circuits in order that the d-c level of the output circuit might accommodate d-c coupling to other circuits (Fig. 22). This may be found valuable when the monostable circuit is used to drive certain direct coupled circuits.

Frequently, discrimination against spurious signals is more important than trigger sensitivity. In that event the emitter of the transistor may be current-biased to insure that the transistor remains in its low-conduction quiescent state until a trigger pulse exceeding a prescribed level is applied. Two current-bias arrangements, and their effects on the emitter input characteristic, are shown in Fig. 23. The high resistance R , in each case, allows a negative current to flow into the emitter when the transistor is in its quiescent state. The presence of the resistance has little effect on operation of the circuit when the transistor is in its active state.

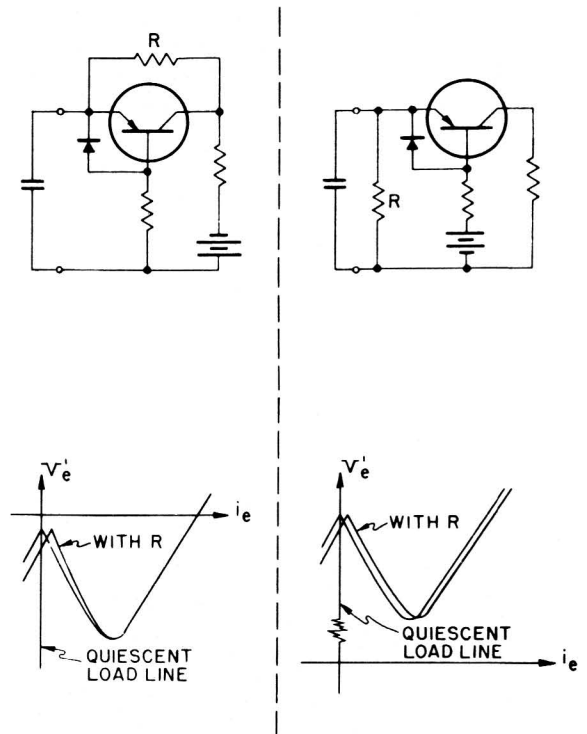


Fig. 23 - Effects of emitter current - bias.

As mentioned in Part I the output waveform of a monostable circuit may be precisely controlled by employing a transmission line, instead of a condenser, as the emitter load.

As illustrated in Fig. 12 the transmission-line controlled circuit keeps the width of the output pulse constant irrespective of individual difference in transistor units. This arrangement is of particular interest in some computer systems where pulse width and pulse delay time have to be precisely controlled.

Bistable Circuits

The basic bistable circuit, shown in Fig. 13, requires that the emitter load line intersect the v'_e-i_e curve once in each region.^{4,8} A study of a number of transistors operating in a typical bistable circuit reveals that the v'_e-i_e curve for a given transistor may lie anywhere within the shaded area of Fig. 24b. In order to insure three-point-intersection for all v'_e-i_e curves within the area, R_e must be small and the values of E_{ee} must lie between E_1 and E_2 . Since the emitter usually serves as an input terminal for triggering, a low value of R_e implies a low input impedance, while the required value of E_{ee} may make the circuit unreliable under adverse conditions.

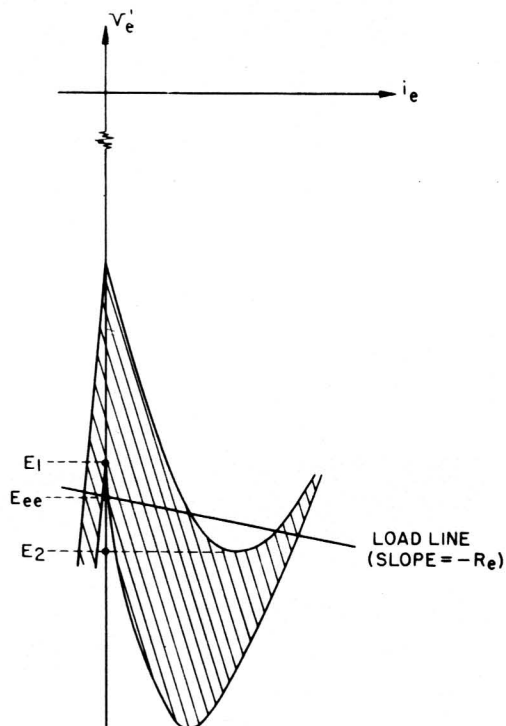
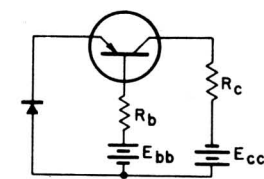
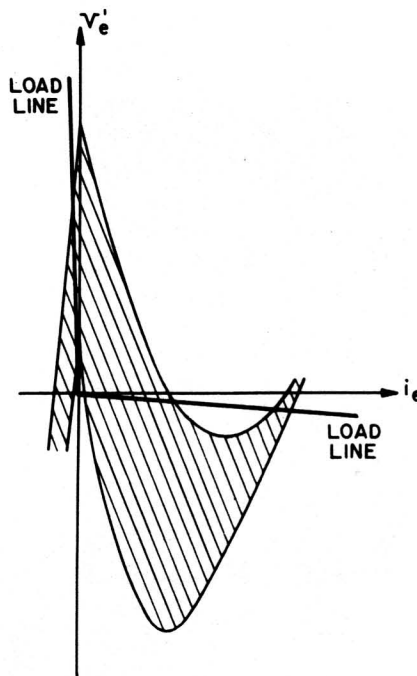


Fig. 24 - Emitter input characteristics of basic bistable circuit.



(a) Circuit arrangement.



(b) Emitter input characteristics.

Fig. 25 - Practical bistable circuit.

A practical single transistor bistable circuit using a non-linear resistance as the emitter load is shown in Fig. 25a. A base voltage bias E_{bb} is used to eliminate the use of the critical emitter bias E_{ee} . The circuit parameters are so chosen that, for the majority of transistors, the center portion of the negative resistance region of each v'_e-i_e curve lies on the i_e axis. A crystal diode is used as the emitter load, causing the emitter load line to have two straight portions as shown in Fig. 25b. This non-linear load line insures the three-point-intersection requirement for each v'_e-i_e curve. Furthermore, at the low conduction state the direction of emitter current is such that the back-resistance of the crystal diode constitutes a high impedance. Thus the input impedance of the circuit is high in its OFF state; and the circuit may be readily triggered into its ON state by the application of a small positive pulse at the emitter.

Any change in circuit parameters and transistor characteristics affects the shape of the v'_e-i_e curve; and a large departure from the designed value may render the circuit inoperative. However, the circuit parameters in the practical circuit are much less critical than are the values of E_{ee} and R_e in the basic bistable circuit, especially when E_{ee} and E_{cc} are from the same power supply. Laboratory experience revealed that the practical circuit is highly stable; and reliable operation was observed even when power dissipation within the transistor was high enough to cause heating of the unit. The single-transistor circuit, in fact, was found superior even to earlier twin-transistor bistable circuits in which reliability had been emphasized.

A Decade Counter

To illustrate the practical application of point-contact type transistors in pulse circuits, an all-transistor decade counter will be described here (Fig. 26). The counter takes the form of a conventional transfer-pulse ring counter. Each decade of the counter consists of ten bistable units inter-connected to form a closed ring. One of the ten bistable units is in the ON state while the remaining nine units are in the OFF state. An input counting pulse, fed to all the bistable units in parallel, tends to turn all the units to the OFF state.

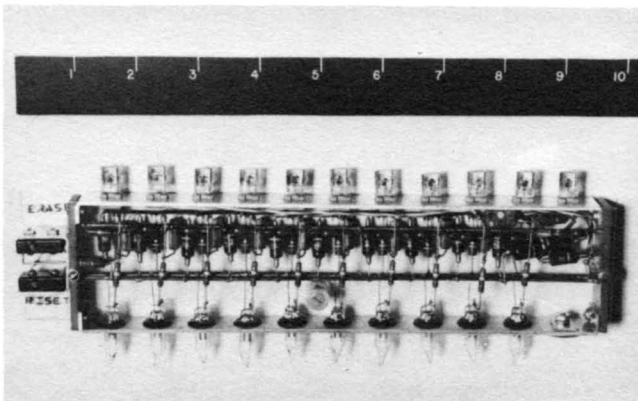


Fig. 26 - Transistor decade counter.

When the originally ON unit jumps to its normal state it sends out a transfer pulse which overrides the input pulse at the next succeeding

unit and turns the latter to the ON state. Successive input pulses will advance the ON state along the ring in the same manner. The neon lamps shown in the photograph are connected so as to indicate which unit is in the ON state, and thus indicate the count.

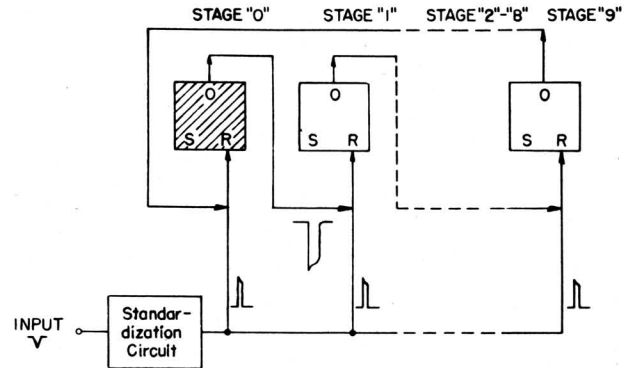


Fig. 27 - Block diagram of transistor decade counter.

A block diagram of one decade of the counter is shown in Fig. 27. Before operation, all units save the first are reset to their OFF state. In order to take care of counting pulses of varied width and amplitude a pulse standardization stage is included. The single transistor bistable circuit described in the last section is used as the bistable unit. However, since the emitter is not used as an input terminal at any time, instead of the employment of a crystal diode, the emitter is directly connected to ground, as shown in Fig. 28. The complete wiring diagram is given in Fig. 29.

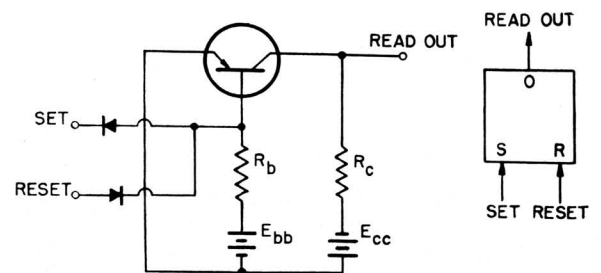


Fig. 28 - A bistable unit.

The laboratory model of the counter was operated at rates of higher than 50,000 counts per second. One decade of the counter has a total power consumption of less than 2 watts. Its physical dimensions are 10 inches x 3 inches x 3/4 inch and it weighs 8 ounces. A vacuum tube decade of comparable performance requires 10 twin-triodes, 2 pentodes, and a power consumption of 60 watts.

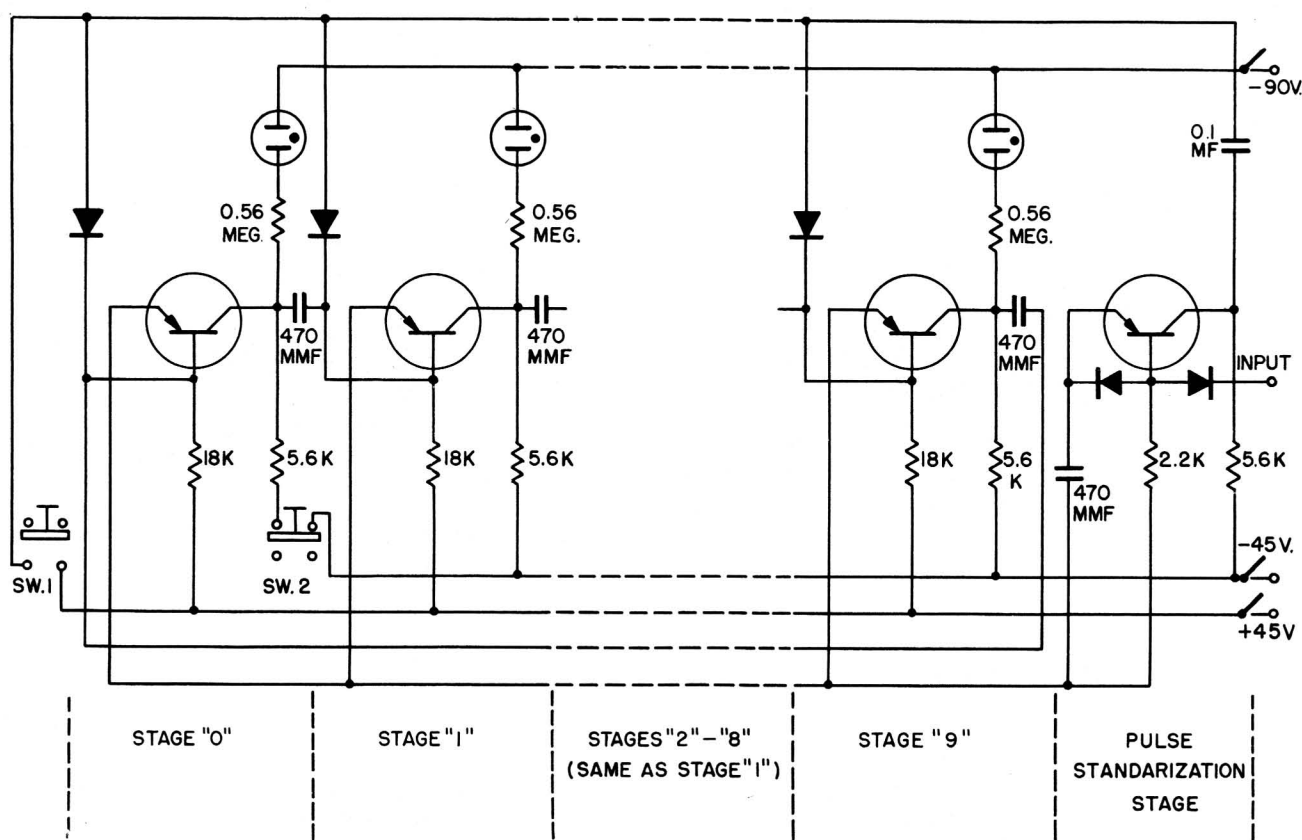


Fig. 29 - Circuit diagram of transistor decade counter.

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- ⁹First investigated by R. O. Endres of RCA Victor Company.