LB-1070

A TRANSISTORIZED HORIZONTAL-DEFLECTION SYSTEM

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Approved

Stuart W. Seeley

A Transistorized Horizontal-Deflection System

The good switching characteristics of junction transistors make them basically well suited to the generation of horizontal-deflection current in television receivers. A completely transistorized developmental horizontal-deflection system is described consisting of an oscillator, driver, output stage with ultor supply, and phase detector. Experimentally, 90-degree deflection at 10 kv has been achieved with the use of selected audio-type power transistors in the output stage. To achieve this deflection it was necessary to operate these transistors beyond the manufacturer's current and voltage ratings. The results demonstrate the feasibility of the circuits and indicate the characteristics that would be desirable in an output transistor designed specifically for this application. In particular, expressions are given for the effect of output transistor switching power capability, saturation resistance, and cut-off time on the circuit performance.

Introduction

The developmental horizontal-deflection system described in this bulletin is shown in block diagram form in Fig. 1. A pulse waveform at horizontal scanning frequency is developed in the horizontal oscillator, amplified by the driver, and applied to the deflection output stage. The output stage delivers a sawtooth current waveform to the horizontal winding of the deflection yoke and also supplies a high-amplitude flyback pulse which can be rectified to produce kinescope ultor voltage. A signal from the output stage is fed back to the phase detector where its phase is compared with that of incoming sync. The resulting error voltage is passed through an integrating circuit and used to control the oscillator frequency and phase.

Basic Output Circuit

In considering the system, it seems best to begin with the output stage since the reactive power required from it can be determined from measurements on conventional (vacuum tube) television receivers. The output requirements of the preceding stages depend in turn on the drive requirements of the output stage. There are several methods by which a transistor might be used to develop a sawtooth deflection current. For example, it might be used, with suitable impedance changes, in the same manner that a tube is normally used for deflection in a television receiver. In this system a damper diode conducts the current during the first portion of scan and the output tube is used as a controlled impedance element to control the current during the completion of scan.

Another method has been described by Guggi[1] in which energy is fed into the yoke during retrace and a large capacitance switched into the circuit to control the current during forward scan. The basic circuit to be discussed here represents a third method which is simple in structure and potentially very efficient with respect to the power dissipated in the output transistor.

It has been shown[2] that a linear sawtooth current can be achieved in an inductance shunted by a capacitance with the use of a voltage source and a bidirectional resistanceless or ideal switch as shown in Fig. 2. If switch S is closed at time T_1, the current will increase linearly according to

$$\frac{di}{dt} = \frac{E_{CC}}{L_1} \qquad (1)$$

until the switch is opened at time t_2. The current then flowing in L_1 will discharge through C_1 in an oscillatory manner. If S is then closed after one-half cycle of free oscillation, the reverse current flowing in L_1 will flow into the power supply, decreasing linearly to zero at t_1. The cycle then repeats.

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[1] W. B. Guggi, "Retrace Driver Deflection Circuit," *IRE Transactions on Broadcast and Television Receivers*, vol. BTR-2, pp. 65-68, October 1956.

[2] G. C. Sziklai, "Current Oscillator for Television Sweep," *ELECTRONICS*, vol. 19, pp. 120-123, September 1946.

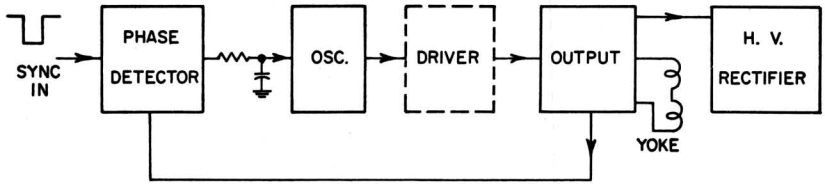

Fig. 1 – Block diagram of horizontal deflection system.

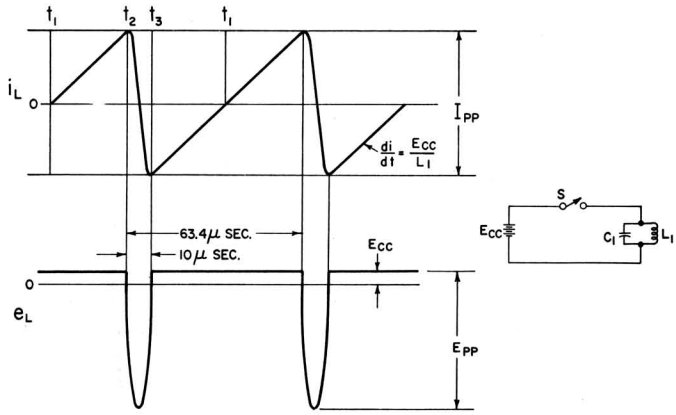

Fig. 2 – Basic output circuit and waveforms.

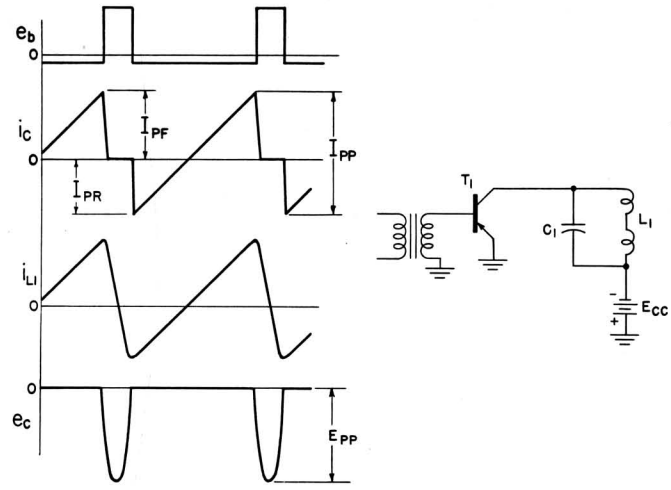

Fig. 3 – Basic transistor output circuit and waveforms.

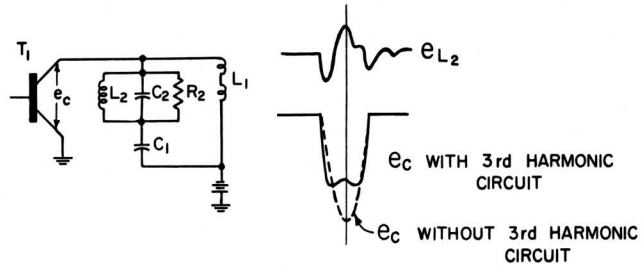

Fig. 4 – Reduction of flyback peak with 3rd harmonic circuit.

In this analysis it was assumed that switch S has negligible resistance to currents flowing in either direction. With the advent of the junction transistor, Sziklai discovered that it can be operated to provide a reasonable approximation to the required switch.[3] It will pass current bi-directionally between emitter and collector. When the transistor is saturated, the emitter-to-collector resistance is a fraction of an ohm; when it is cut off this resistance may be in the megohms. The basic output circuit incorporating a transistor is shown in Fig. 3, together with the corresponding waveforms. The operation is analogous to that of Fig. 2. During scan the base of T_1 is biased sufficiently in the forward direction to place the transistor in saturation. At the end of scan the base is driven in the reverse direction by the applied drive signal, cutting off T_1, while L_1C_1 goes through a half cycle of free oscillation. C_1 is chosen to give a desired return time with the particular yoke inductance employed.

During this flyback interval a relatively large voltage pulse appears on the collector. The yoke inductance must be adjusted so that the peak voltage does not exceed the collector breakdown voltage. At the end of the base pulse, which should coincide with the completion of flyback, T_1 conduction is restored for the next scanning period. The peak T_1 collector current reached prior to flyback is in the normal or forward direction and is designated I_{pf} as indicated in Fig. 3. The reverse peak following flyback is termed I_{pr} and the peak-to-peak collector current, I_{pp}.

[3]LB-906, *"Symmetrical Properties of Transistors and Their Application"* by G. C. Sziklai.

Fig. 4 illustrates a method of reducing the flyback voltage pulse on the collector. L_2C_2 is tuned approximately to an odd harmonic of the flyback frequency--in this case the third harmonic. The voltage e_{L_2} across L_2C_2 is a damped sine wave of third-harmonic frequency which is initiated by the front edge of the flyback pulse. This voltage is 180 degrees out of phase with the voltage across C_1 at the center of the flyback pulse and thus reduces the peak collector voltage about 30 percent. The shape of the resulting collector pulse e_C is indicated by the solid line waveform in Fig. 4.

When a high-voltage winding is placed on the horizontal-output transformer, a similar result can be achieved with a design such that the distributed capacity and leakage inductance resonate at an odd harmonic of the flyback frequency. This has become common practice in television receivers employing vacuum tubes.

Switching-Power Requirements

It is now of interest to determine the desired specifications on the output switching device, i.e., the output transistor. For this purpose assume an example of deflecting a 90 degree kinescope with a 10-kv ultor voltage. The results can be extrapolated for other deflection angles and ultor voltage.

It is evident that for a given yoke geometry and ultor voltage the deflection angle D will be proportional to the peak-to-peak ampere turns in the horizontal winding.

$$D \propto I_{pp}\, N \propto I_{pp} \sqrt{L} \tag{2}$$

where I_{pp} = peak-to-peak yoke current
N = number of turns in yoke winding
L = yoke inductance

Further, for a given return time and flyback pulse shape

$$E_{pp} \propto L\, I_{pp} \tag{3}$$

where E_{pp} = peak-to-peak yoke voltage during scanning cycle.

Then from Eqs. (2) and (3)

$$D \propto (I_{pp} E_{pp})^{1/2} \tag{4}$$

Thus, the deflection that can be achieved with a particular transistor is determined by the product of its peak-to-peak current handling capability times the peak voltage it can withstand. This represents the bidirectional switching power capability. The bidirectional switching power employed in a vacuum-tube television receiver with a 90-degree kinescope and a 10-kv ultor supply has been measured at 1300 v.a. This value has been confirmed with measurements on a transistor deflection stage. Selected transistors of commercially-available types have been found which are capable of this switching power, although such operation is beyond the manufacturers' ratings on peak voltage and current.

For a given flyback waveshape the voltage pulse applied to the collector during flyback is proportional to the inductance seen from the collector. If the yoke is direct-coupled, this is the yoke inductance itself; if transformer coupling is used, the inductance reflected to the collector determines the voltage. To obtain full advantage of the switching power capabilities of a transistor, this inductance should be such that the maximum safe pulse voltage is developed on the collector when the desired deflection has been achieved. With a fixed retrace pulse shape and return time, there is a fixed ratio between the flyback pulse amplitude and the supply voltage E_{cc}. With a 9-μsec retrace time and third harmonic cancellation, this relationship is

$$E_{pp} \approx 10\, E_{cc} \tag{5}$$

Because the drive requirement for the output transistor decreases with the collector current to be controlled, and because the power-supply filter cost tends to decrease for higher load impedances, it seems desirable to have transistors with higher breakdown voltages than are now available. The collector junction breakdown and punch-through voltages determine the maximum permissible collector peak voltage. There is little tendency for the output stage to "run away" because of the switch-type mode of operation. During forward scan, collector current is controlled by the load circuit; during retrace the base is reverse biased so that the collector current is limited to the I_{co} value of the collector junction.

When the deflection power and maximum voltage are specified, the peak-to-peak current to be handled is automatically determined. Thus, if the required switching power is 1300 v.a. and the safe collector voltage is 130 volts, the peak-to-peak current is 10 amps. In any practical circuit this current swing will be greater in one direction than in the other. The yoke energy following retrace is that which was in the system prior to retrace less the flyback losses and energy delivered to the ultor supply. The dissymmetry is thus a function of the ratio of dissipated to stored energy in the system. Typically, the current might be 60 percent in the forward direction, 40 percent in the reverse direction as illustrated in Fig. 3.

Transistor Saturation Resistance

The series saturation resistance R_S that can be tolerated between emitter and collector during forward scan is a function of the resulting non-linearity which is acceptable. In a purely inductive circuit, the current will increase linearly as indicated in Eq. (1). Any resistance in the circuit will result in a sawtooth voltage component being added to the applied voltage E_{cc}. The variation of the deflection current slope from edge to edge is in proportion to the variable component added to E_{cc}. Thus R_S results in linearity distortion from edge to edge, as follows:

$$\text{Percent non-linearity} = \frac{I_{pp}\, R_S}{E_{cc}} \times 100 \tag{6}$$

This non-linearity will be added to others that will arise from other resistances in the circuit, primarily in the yoke winding and, if one is used, in the transformer. In the example where E_{cc} is 13 volts and I_{pp} is 10 amps, if R_S is allowed to contribute a 5 percent non-linearity, Eq. (6) indicates a maximum R_S of 0.065 ohm. Note that since E_{cc} is proportional to the allowable breakdown voltage and I_{pp} is inversely proportional (for a given deflection power), the allowable R_S increases with the square of the permissible collector voltage.

The value of R_S also largely determines the power dissipated in the transistor during forward scan. In the example being considered, if R_S is 0.065 ohm, this dissipation is less than 1 watt.

Switching Time

With presently-available transistors a large portion of the dissipation in the output transistor occurs during collector current cutoff. The collector flyback pulse starts at the beginning of the collector current cutoff interval. It is shown in Fig. 5 that when third harmonic

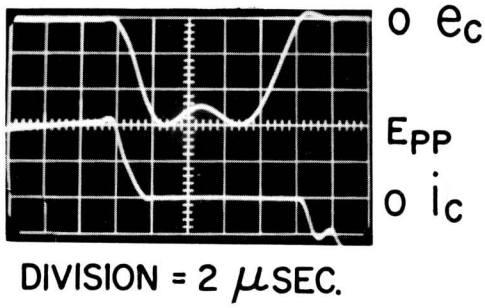

Fig. 5 – Collector voltage and current waveforms during retrace.

cancellation is used with a return time of 10 μsec, the voltage increases approximately linearly to the value E_{pp} in 3 μsec. To calculate the transistor dissipation during cutoff, it is assumed that the current cutoff and voltage build-up are linear. From the waveforms of Fig. 5, this approximation seems reasonable. Thus during the cutoff interval,

$$e_c \approx \frac{t}{3} E_{pp} \qquad when\ t < 3\ \mu sec \tag{7}$$

$$i_c \approx I_{pf}\left(1 - \frac{t}{T_{co}}\right) \quad when\ t \leq T_{co} \tag{8}$$

where t = time from beginning of cutoff in μsec
T_{co} = time required for i_c cutoff in μsec

Dividing the energy dissipated during cutoff by the duration of a horizontal period gives the average collector power dissipation due to cutoff, P_{co}.

$$P_{co} = \frac{1}{63.4} \int_{t=0}^{t=T_{co}} i_c e_c\, dt \approx \frac{T_{co}^2}{1140} E_{pp} I_{pf} \tag{9}$$

where I_{pf} = peak collector current prior to flyback

This expression is approximately correct for cutoff times up to 3 μsec. In the chosen example, if I_{pf} is 6 amps, the average dissipation due to cutoff is 0.69 watt when T_{co} is 1 μsec and varies with square of T_{co}. The desirability of minimizing cutoff time is obvious.

Static Characteristics Of Present Power Transistors

One pertinent characteristic that is usually not given by the manufacturers of power transistors is the bilateral collector-emitter characteristic in the saturation region. As an example, Fig. 6 shows such a characteristic for an RCA type 2N301A power transistor. Collector-emitter voltage vs collector current is shown for several values of forward base-to-emitter voltage. It will be noted that the saturation resistance is lower and remains low over a wider range with higher values of base bias. This resistance reaches an average of 0.05 ohm over the 8-amp peak-to-peak current range plotted. Constant base voltages were used in Fig. 6 because in the operating circuit a low-impedance driving source is used. However, the forward driving power depends on the input resistance when the transistor is in the saturated state and on the base current required to maintain that state. The minimum base current required to maintain saturation during the last half of scan is

$$I_{bmin} = \frac{I_{pf}}{\beta} \tag{10}$$

where β = base-collector current gain at I_{pf}.

As noted, the saturation resistance will be less if a base current in excess of I_{bmin} is used during scan.

The fact that the reverse collector current peak I_{pr} is approximately 40 percent of the peak-to-peak current swing I_{pp} indicates the desirability of using an output transistor with approximately symmetrical current gains to maintain saturation during the first half of scan. In practice, the forward base voltage applied during scan

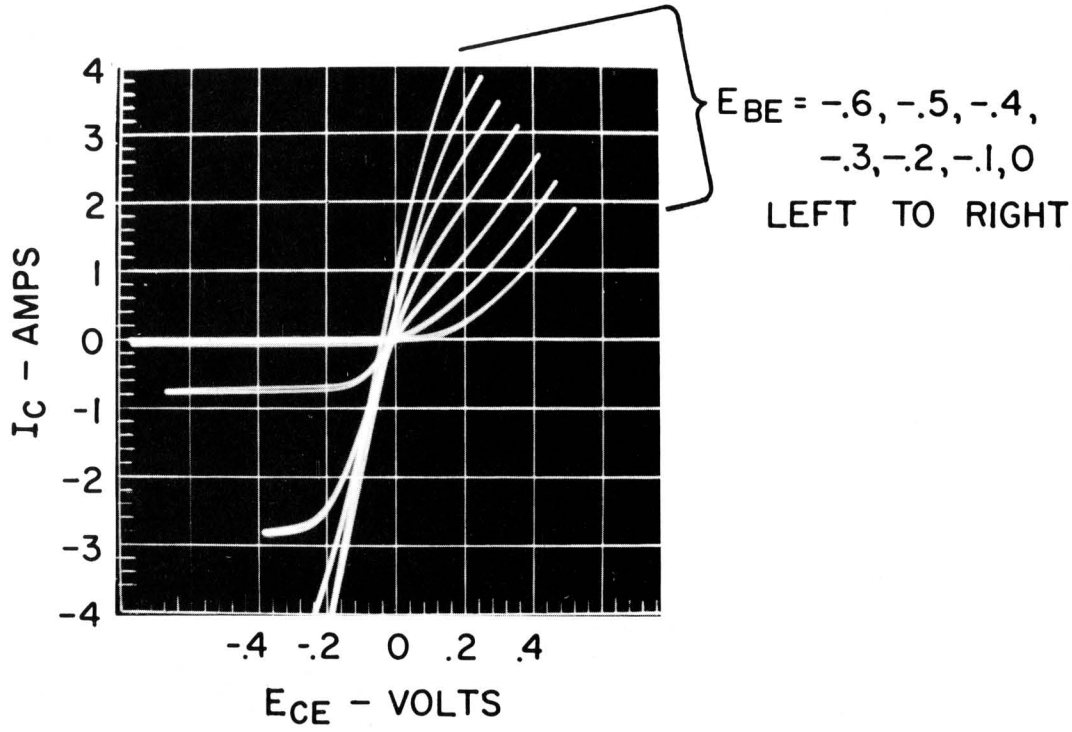

Fig. 6 – Bilateral saturated collector characteristic.

may have some slope due to lack of low-frequency response in the driving transformer. This slope is in a direction to increase the relative base current during the first portion of scan and thus decreases to a degree the relative reverse direction current gain required. If a highly unsymmetrical transistor is used, a diode can be placed in shunt with the transistor to carry the current in the reverse direction.

Cutoff Behavior Of Present Power Transistors

Existing commercial power transistors in general have not been designed for rapid switching, and they turn off more slowly than is desirable in the horizontal-deflection application. Nevertheless, with proper drive, such units will function in the circuit described. If one were to attempt to cut off a collector current of several amperes in a typical power transistor by merely reducing the forward base bias to zero, the cutoff time would be many times the total permissible flyback time. However, if the cutoff pulse applied to the base is of sufficient amplitude to bias it in the reverse direction with respect to the emitter, a transient reverse base current will flow as stored minority carriers are removed from the base layer and the collector current cutoff time will be reduced. The cutoff time has been found to vary approximately in proportion to the peak collector current and in inverse proportion to the applied reverse base bias. The base and collector waveshapes during cutoff are shown in Fig. 7. The interval between the initial application of the cutoff pulse to the base and the completion of collector current cutoff has two components--the *storage time* T_S, during which the transistor remains saturated and continues to act like a closed switch, and the *cutoff time* T_{CO}, which represents the interval of collector current decay.

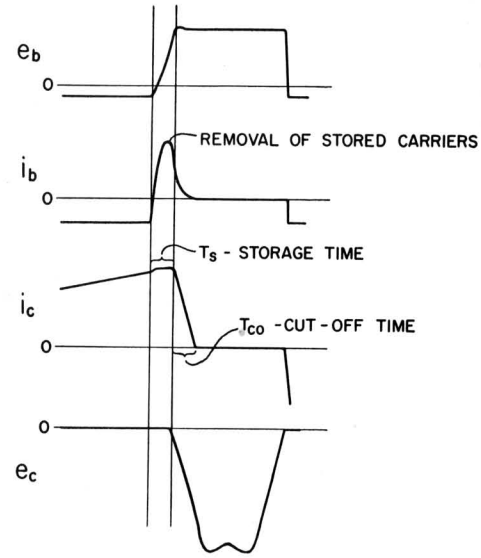

Fig. 7 – Base and collector waveforms during cutoff.

The duration of T_S is essentially zero when the base current during scan has the value I_{bmin} but may increase

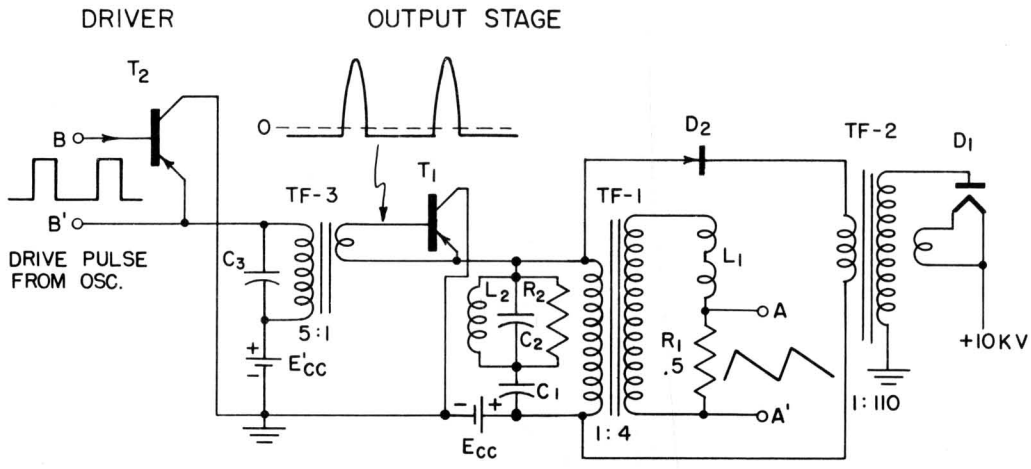

Fig. 8 – Output stage and driver.

to several microseconds with higher levels of base current. In a sync-driven deflection system, T_S will introduce a time delay, but in the automatic phase control system to be described, the oscillator phasing will automatically shift to eliminate any phase discrepancy of the output deflection current with respect to sync. As long as the saturation resistance remains low during the storage interval, the duration of this interval has no serious effect on the system.

The collector flyback pulse builds up during the cutoff interval T_{CO}. The importance of minimizing T_{CO} has already been discussed. To make presently available power transistors cut off as rapidly as practically possible, a reverse base pulse on the order of 10 volts has been employed. Depending on the output transistor used, up to several amperes of reverse base current may flow during the cutoff process and a peak drive power as high as 40 watts may be required to achieve a cutoff time on the order of 3 μsec. When inherently faster transistors with the required switching capacity are developed, it is anticipated that the peak drive power required will be much less.

Developmental Output Stage

A developmental deflection and high-voltage output circuit is shown in Fig. 8. A bootstrap output circuit is used so that the transistor collector and case can be grounded for best heat conduction. A 1-mh yoke is used with transformer TF1 which reflects an inductance of 62 μh at the transistor T_1. High voltage is taken from transformer TF2 which reflects an inductance of 400 μh at the transistor. C_1 tunes the reflected inductance to produce the desired flyback period. L_2C_2 provides third harmonic cancellation as previously described. Diode D_2 opens during scan and prevents damped oscillatory voltages in TF2 from causing "ripples" in the deflection current. An oscillogram of the output current in the deflection yoke is shown in Fig. 9.

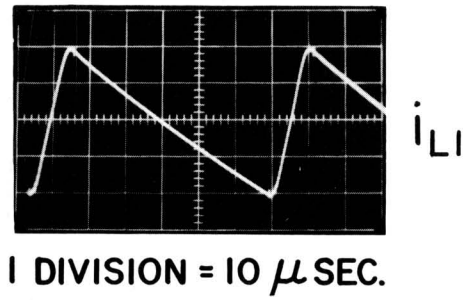

Fig. 9 – Deflection yoke current.

A voltage reference of the deflection current appears across sampling resistor R_1. This signal is applied to the phase detector which will be discussed later. The 1.2-volt peak-to-peak sawtooth voltage developed across R_1 has about a 2 percent effect on linearity. If a lower impedance yoke were used, this effect would become more serious because the sawtooth component would represent a greater proportion of the voltage across the yoke during scan.

Driver Stage

The relatively large amount of drive power needed to make present power transistors cut off sufficiently fast makes the use of a driver stage T_2 desirable, as shown in Fig. 8. This stage is operated in the same manner as described for the basic output stage. It is saturated during scan and cut off by a pulse from the oscillator during retrace. During retrace a pulse analogous to the flyback pulse appears across the primary of TF3. This pulse, after being stepped down in voltage to reduce the circuit impedance, is used to cut off the output stage. The pulse

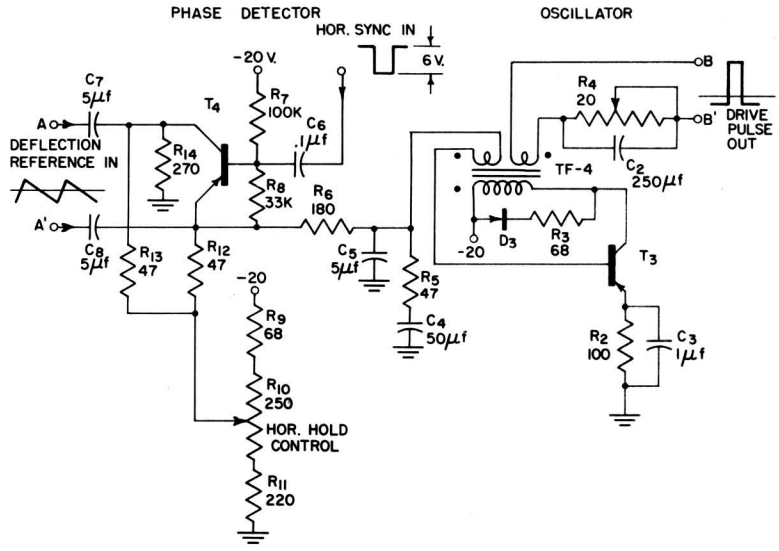

Fig. 10 – Oscillator and phase detector.

has the shape of one-half a sine-wave cycle. One might think that a steeper-front pulse would produce faster cutoff of the output current; however, this is not necessarily true. If the output stage is operated with sufficient forward bias to produce a storage time of a few microseconds, the cutoff pulse will be close to its full amplitude during the cutoff interval. It is during this interval that carriers should be removed as rapidly as possible to reduce the cutoff time.

AC coupling the drive signal results in a d-c axis about 10 percent above the signal level during scan, as indicated by the T_1 base waveform shown in Fig. 8. Thus a forward bias equal to about one-tenth the peak-to-peak drive amplitude is applied to the T_1 base. This eliminates the need for an added bias supply and protects the output stage in case of drive failure. When faster deflection output transistors become available, it seems probable that the driver stage can be eliminated.

Oscillator Stage

The horizontal oscillator and phase detector circuits are shown in Fig. 10. The oscillator is of the blocking type in which T_3 is saturated during flyback and cut off during scan. This on-off mode of operation results in relatively high peak output compared with the transistor dissipated power. Much of the dissipation occurs on the transitions between the off and saturated states, so that the transition intervals should be brief. Since this stage must supply its own drive and drive the following stage as well, the oscillator transistor needs more high-frequency gain than is possessed by the type used in the output stage. The maximum peak output from the oscillator is proportional to its switching power capability. The transistor used is an experimental type with a maximum oscillation frequency on the order of 10 mc, a maximum collector voltage of 35 volts, and a peak current rating of 0.5 amp.

The oscillator collector voltage and current waveforms are shown in Figs. 11a and 11b respectively, with the oscillator loaded by the driver stage. The oscillator transition intervals between on and off states vary many-fold with loading, being longer when the load is heavy. The output waveform applied to the driver stage as shown in Fig. 11c is about 6 volts in amplitude. The peak power delivered is about 2 watts. The fact that the load is non-linear limits the power that can be delivered to the driver, because the impedance match must be compromised to accommodate the low base impedance offered during the forward-scan portion of the cycle and the higher base impedance existing during the retrace portion of the cycle. The oscillator repetition frequency and pulse width depend primarily on the load, R_2, C_3 and the ratio of T_3 base bias to collector supply voltage, (Fig. 10). For a given load, adjustment of the other three factors gives a wide range of control over the repetition frequency and pulse duty factor. The base and emitter voltage waveforms which determine the oscillator timing are shown in Fig. 11d. In operation the oscillator frequency is controlled by the base bias, which is determined by the hold control setting and phase detector output.

Diode D_3 (Fig. 10) serves to limit the transformer inductive overshoot during turn-off so that the collector breakdown voltage is not exceeded. The output signal to be applied to the following stage is taken from a third winding on the oscillator transformer. Forward bias for the driver is obtained by a-c coupling the input signal in the same manner as on the output stage. Since the for-

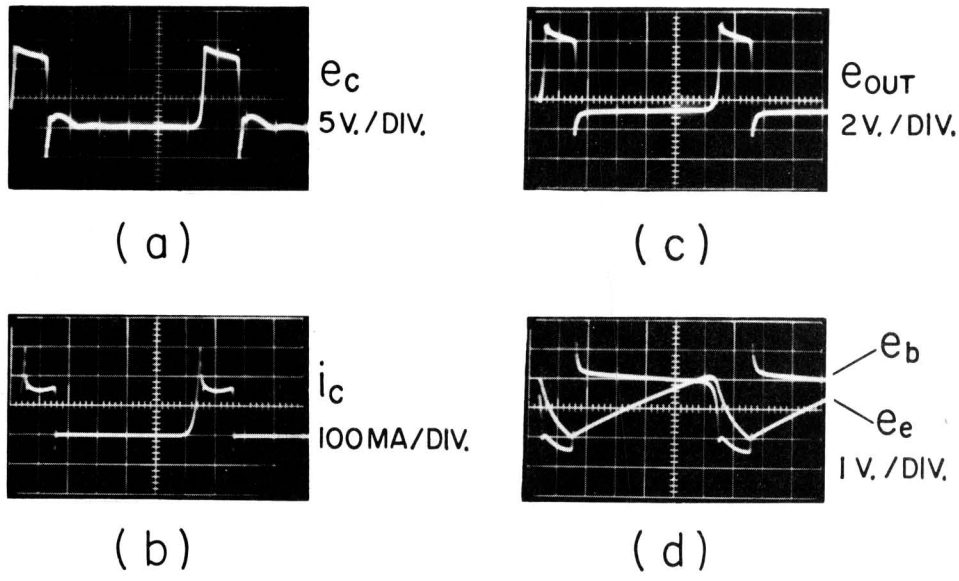

Fig. 11 – Oscillator waveforms.

ward bias tends to be greater than is required, the operating point is shifted somewhat in the reverse direction by bias resistor R_4 (Fig. 10).

Phase Detector

In Fig. 10 transistor T_4, which is a symmetrical p-n-p type, functions as a horizontal phase detector.[4] The signal developed across R_1 (Fig. 8), which corresponds to the deflection current sawtooth waveform, is applied between emitter and collector of T_4. Negative sync pulses applied to the base of T_4 permit emitter-collector current to flow during the sync interval, while self-bias developed by base current flow through R_8 keeps the transistor cut off between sync pulses. When the horizontal system is properly phased, the duration of retrace will overlap the sync interval. As indicated by the waveform shown in Fig. 10, the collector-to-emitter voltage of T_4 is negative during the first portion of retrace and positive during the last portion. The instantaneous direction of emitter-collector current flow during the sync pulse is determined by this polarity.

[4]Ibid

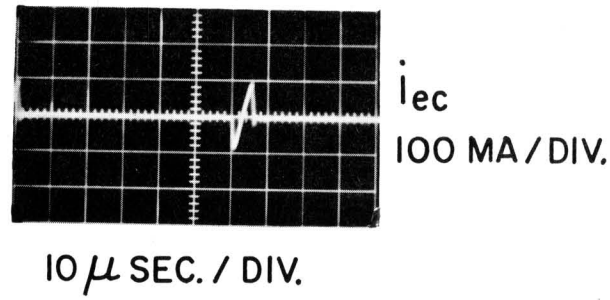

Fig. 12 – Phase detector current.

This current is shown in Fig. 12 for the case where retrace is approximately centered on sync. The integrated voltage output under this condition is essentially zero. If the phasing shifts, the current flow becomes unsymmetrical and a d-c component is developed across R_{12} (Fig. 10). This error signal is applied through the anti-hunt integrating circuit $R_6C_4C_5R_5$ to the oscillator base winding and acts to oppose the original phasing error. The frequency sensitivity of the oscillator to changes in base bias is on the order of 2000 cycles/volt. The impedance of the phase detector is made relatively low to reduce the d-c internal error voltage drops due to oscillator base current flow. This current is about 20 ma average. The pull-in range of the system is on the order of ±200 cycles.

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