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A MONOSTABLE MULTIVIBRATOR CIRCUIT USING COMPLEMENTARY TRANSISTORS

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Approved

Stuart Wm. Seeley.

A Monostable Multivibrator Circuit Using Complementary Transistors

A transistor monostable circuit using complementary transistors is described. Using this unique property of transistors in this application results in certain advantages compared to the transistor monostable circuit directly analogous to a tube monostable multivibrator. These are: (1) higher inherent charge to discharge ratio (i.e., faster recovery time) for the timing capacitor; (2) both transistors are off during the timing cycle providing relative circuit insensitivity to transistor variation. An analysis of circuit operation and timing is given, and the effects of temperature on circuit reliability are discussed.

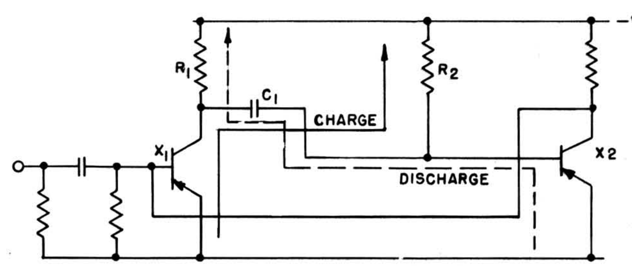
The circuit has operated reliably with input frequencies from 250 cycles to one megacycle. With proper attention to component and supply voltage tolerances and using a silicon PNP transistor, operation without manual adjustments can be obtained from -50 to +70 degrees C. A typical application for this circuit would be in the divide counters in television synchronizing generators.

Introduction

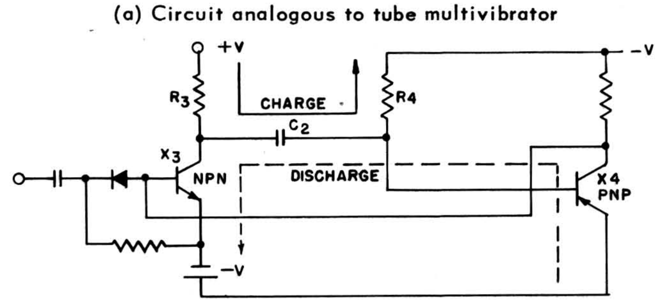
Multivibrators of the monostable type are characterized by a biasing condition where both amplifier elements are in a particular stable state in the absence of an external trigger. An input trigger changes this state, and after a predetermined length of time the circuit returns to the stable state. This circuit can be used to produce output pulses of a controlled width in response to input pulses, or as a counter, by accepting a number of input trigger without action during the timing cycle.

The timing period for the monostable circuit can be divided into two phases. The first phase occurs from the introduction of an input trigger to the point when the voltage on the timing capacitor changes from its initial value to a value which starts the circuit back to the stable state. In the second phase, generally referred to as the recovery, the timing elements discharge to the values corresponding to the stable condition. A high charge-to-discharge ratio is desirable because unreliable operation can occur if an input trigger occurs when the timing elements are discharging.

The fact that transistors have NPN and PNP types, compared to a single polarity type for tubes, allows a monostable circuit to be connected two ways as shown in Fig. 1. Fig. 1(a) is analogous to the tube monostable circuit, while 1(b) is the complementary symmetry monostable circuit which is the subject of this bulletin. The charge and discharge paths of the circuits are shown. For Fig. 1(a) the charge path is R_2C_1, and the discharge path is C_1 through R_1 and the input resistance of *X-2* in series. For Fig. 1(b) the charge path is $(R_3 + R_4)\ C_2$ while the discharge of C_2 occurs through a low resistance comprising the input resistance of *X-4* and the saturation resistance of *X-3*. The inherent charge to discharge ratio of circuit 1(b) is greater than the tube analogue in 1(a) in a working circuit.



(a) Circuit analogous to tube multivibrator



(b) Complementary symmetry multivibrator

Fig. 1 – Comparing capacitor charge and discharge paths for conventional and complementary symmetry monostable multivibrator.

Description of Operation

Referring to Fig. 2, the operation of the circuit is outlined as follows. In the absence of an input trigger to C_2:

(1) Current in R_5 due to V_2 biases *X-2 on.*

(2) *X-1* is biased *on* also by the current in the series loop comprising V_3, the saturation resistance of *X-2*, R_3, and the base-emitter circuit of *X-1*. With *X-1* and *X-2* on, a negative or differentiated positive input trigger is applied to C_2.

(3) This turns *X-1* off causing the voltage at 1 to go to slightly less than V_1.* Since the voltage across C_1 cannot change instantaneously this positive voltage appears at point 2, the base of *X-2*, turning *X-2 off*.

(4) C_1 now charges towards the negative voltage V_2 through $R_2 + R_5$.

(5) When the voltage at 2 becomes slightly negative and approaches V_{be2} (base-emitter voltage on *X-2* for saturation) *X-2* saturates and by amplifier action turns *X-1* on also.

(6) C_1 now discharges through a path comprising the saturation resistance of *X-1* and the input resistance of *X-2*.

(7) Both *X-1* and *X-2* are now on and ready for another input trigger to start recycling.

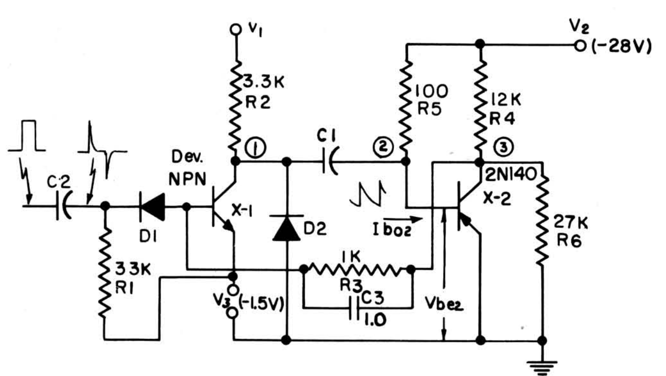


Fig. 2 – Monostable multivibrator circuit.

Frequency division with the circuit is accomplished by controlling the length of time *X-1* and *X-2* are off so that a specified number of input triggers can be accepted without causing circuit action.

High charge to discharge ratio and arranging for both transistors to be off during the timing period, are the two major advantages of this circuit compared to the transistor analogue of the vacuum tube monostable counter circuit.

*See appendix for detailed analysis of this interval.

Temperature Effects

Two main temperature effects are present in the circuit; one is component variations with temperature, the other is the temperature effects in the transistors, principally that due to the PNP unit. The effect of component and temperature variations on the charge time is given in Eq. (1) in the appendix. Selecting components with minimum variation with temperature will improve circuit reliability.

At a given temperature, since both transistors are *off*, the timing is determined almost entirely by passive circuit elements. At temperatures above room ambient, however, the reverse base saturation current I_{bo} of the PNP unit which approximately doubles for each 7 degrees C temperature rise, begins to affect the charge time of C_1. The resistance associated with the current generator I_{bo} can be considered in parallel with R_5 and can load R_5 sufficiently at elevated temperatures to appreciably change the charge time of C_1. One means of reducing the effect of I_{bo} is to lower the resistance of R_5, but this is undesirable because it would also reduce the charge to discharge ratio of C_1. A better means of reducing the temperature effects is to use a silicon transistor for *X-2*. The I_{bo} current in the silicon transistor will increase with temperature, but its value at room temperature is at least 100 times less than that for germanium, so that the I_{bo} current (less than $10\mu a$) at elevated temperatures of 70 degrees C will cause a negligible change in the $(R_2 + R_5)$ C_1 time constant.

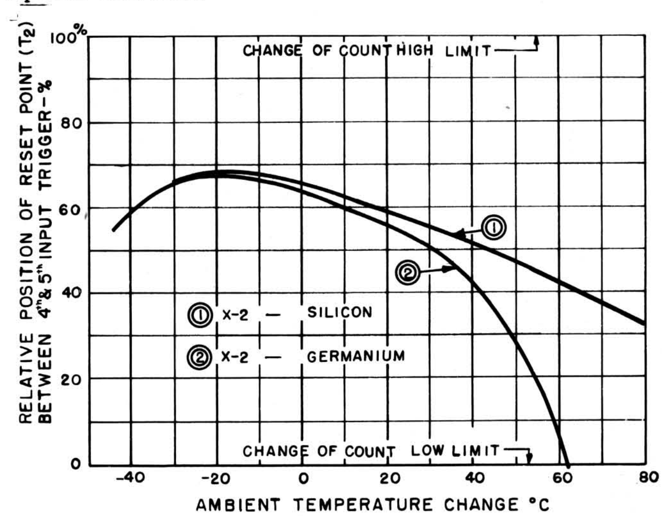
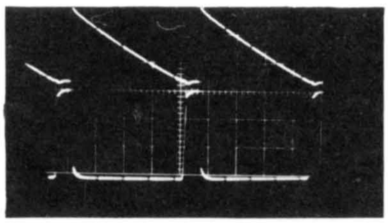


Fig. 3 – Circuit recovery time variation between 4th and 5th input trigger vs temperature when used as a divide-by-five counter.

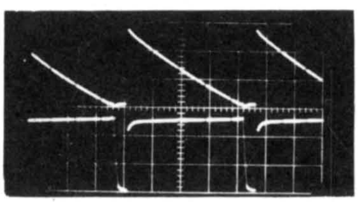
Figure 3 shows the temperature effects on the circuit using silicon or germanium transistors for *X-2*. This curve shows the percentage shift in the position of the reset point of the circuit between the 4th and 5th input trigger as a function temperature. A shift to 0 to 100 percent on the vertical axis indicates a miscount. The improvement obtained by using a silicon transistor is clearly shown.

Performance

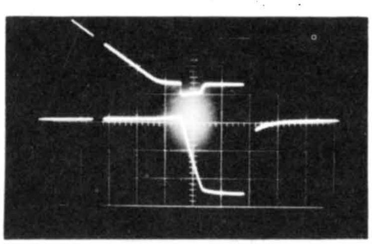
The circuit used as a divide counter will operate reliably with input signals from less than 250 cycles to one megacycle. Fig. 4 shows various waveforms for a



(a) V = 5 volts/div.
H = 1 ms/div.
Top = V_{be2}
Bottom = $V_{collector\,x\text{-}2}$



(b) V = 5 volts/div.
H = 1 ms/div.
Top = V_{be2}
Bottom = $V_{collector\,x\text{-}1}$



(c) Waveshape of (b) expanded
H = 200μs/div.
V_{Top} = 0.5 volts/div.
V_{Bottom} = 5.0 volts/div.

Fig. 4 – Waveforms of circuit used as a divide-by-five counter-frequency input 1030 cps.

1 kc input signal. The recovery voltage at the base of *X-2* for a *1 kc* input signal is intensity modulated by the input signal on the oscilloscope display to show a count-by-five operation. The recovery period and the discharge of C_1 is shown between the 4th and 5th input trigger. An enlarged presentation of this recovery waveform is shown in Fig. 4(c).

A negative going pulse appears at the collector of *X-1* while a positive going pulse appears at *X-2*. The leading edge of the negative pulse has a poorer rise time than the trailing edges. The slope of this leading edge is related to the time required to turn *X-2 on.*

Other Considerations in the Circuit

Besides temperature effects there are two other potential areas of unreliability in the circuit: (1) tendency to free run – that is for the multivibrator to cycle without an input trigger, (2) inability to start the circuit with an applied input trigger. DC stability is insured by resistor R_3 which limits the current due to V_3 flowing through the low saturation resistance of *X-2*. This in turn reduces the bias current through R_5 required to hold *X-2 on.* To determine the minimum d-c current gain of *X-2* to prevent free-running it is necessary to calculate the collector and base current in *X-2*, and divide the collector current by the base current. For example:

Collector current of *X-2*:

$$I_{c2} = \frac{V_2}{R_4} + \frac{V_3}{R_3} = \frac{28}{12} \times 10^{-3} + \frac{1.5}{1} \times 10^{-3} = 3.8\ ma.$$

Base current of *X-2:*

$$I_{b2} = \frac{V_2}{R_5} = \frac{28}{82 \times 10^3} = 0.342\ ma.$$

Minimum d-c current gain of *X-2* for stability:

$$\frac{I_{c2}}{I_{b2}} = \frac{3.8}{0.34} = 11$$

Two components, *D-2*, and R_3 improve starting reliability of the circuit. *D-2* serves to keep *X-1* from going heavily into saturation, and R_3 unloads the input circuit of *X-1*. Both these effects operate to reduce the input current and hence trigger power required to turn *X-1 off.* The circuit will start with a minimum trigger of 0.2 volts.

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Appendix

The time duration from the incidence of an input trigger which turns both transistors *off* to the point when the capacitor C_1 is discharged can be divided into three intervals as shown in Fig. 5

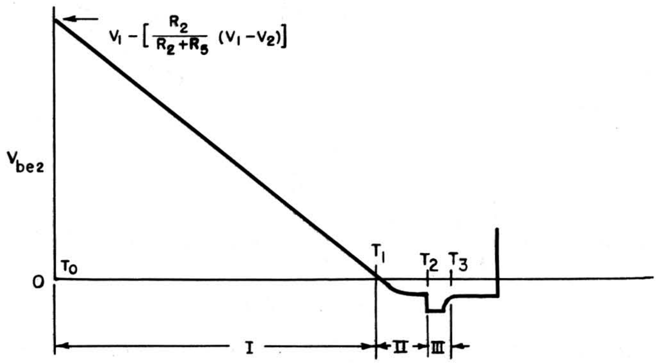


Fig. 5 – Base-emitter recovery voltage of X-2 indicating three portions of timing cycle.

I. Time T_0, when an input trigger is applied, to time T_1, when V_{be_2} becomes zero.

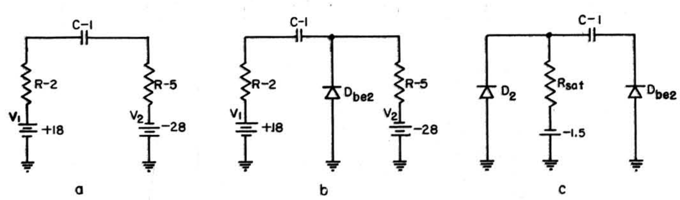
II. Time T_1, from V_{be_2} at zero, to T_2 when V_{be_2} reaches a voltage sufficient to cause *X-2* to saturate.

III. Time T_2, when *X-2* is saturated, to time T_3 when C_1 is fully discharged.

For interval I, the equivalent charging circuit is shown in Fig. 6(a). The time for C_1 to charge to zero volts is given by:

$$T_I = (R_2+R_5)C_1 \ln\left[\frac{V_2 - I_{bo_2}R_5 - V_1 + \left(\frac{R_2}{R_2+R_5}[V_1 - V_2]\right)}{V_2 - I_{bo_2}R_5}\right]$$

For interval II, the equivalent charging circuit is shown in Fig. 6(b). At T_1, the start of this interval, the base-emitter voltage of *X-2* goes negative and *X-2* starts to conduct. The charging current for C_1 is now controlled by the diode of the base-emitter circuit of *X-2* as shown in Fig. 6(b). The time T_2 occurs when the base current of *X-2* is sufficient to cause collector saturation. It is fairly difficult to develop the time duration equation for interval II. The duration of this interval is about 2 percent of the total recovery time; this is within the limits of accuracy of the other factors in the timing equation and can be neglected.



(a) Circuit during interval I.
(b) Circuit during interval II.
(c) Circuit during interval III.

D_{be2} Base-Emitter Circuit X-2
R_{sat} Saturation Resistance X-1

Fig. 6 – Approximate equivalent circuits during recovery of the multivibrator circuit.

For interval III, the equivalent circuit is shown in Fig. 6(c). This is the discharge time for C_1 and constitutes about 2 percent of the total recovery time.

Figure 4(c) shows the interval between the fourth and fifth input trigger on the V_{be_2} recovery voltage with the input triggers used to blank out the display. Intervals II and III and the *X-1* collector waveshape are shown.

References

1. A. C. Luther, Jr., "Stabilization of Pulse Duration in Monostable Multivibrators", *RCA Review*, September, 1955, Volume XVI, No. 3.
2. H. C. Lin and A. A. Barco, "Temperature Effects in Circuits Using Junction Transistors", "Transistors I", *RCA Review*, Princeton, N. J., 1956.