LB-1052

LARGE-AREA GERMANIUM POWER TRANSISTORS

RADIO CORPORATION OF AMERICA

RCA LABORATORIES

INDUSTRY SERVICE LABORATORY

RADIO CORPORATION OF AMERICA

RCA LABORATORIES

INDUSTRY SERVICE LABORATORY

LB-1052

LARGE-AREA GERMANIUM POWER TRANSISTORS

Approved

Large-Area Germanium Power Transistors

Both p-n-p and n-p-n experimental alloyed-junction power transistors have been developed to operate at collector currents of 10 amperes or more. Depending on design factors (polarity, low or high voltage operation) collector-to-base current ratios range up to 200 at 1 ampere and to 60 at 10 amperes. Thermal resistances are about 1 to 2 degrees C per watt. The extension of the operating current range by an order of magnitude has been accomplished by increasing the junction area (0.24-inch diameter). Modifications of conventional alloying techniques were developed to obtain relatively-flat large-area junctions. To reduce the junction curvature, pressure washers having an inverse curvature are used to shape the molten alloy. Base-lead resistance is reduced by a factor of 6 by the use of ring emitters with axial and co-axial base contacts. Because of the transverse field developed in the base, wide variations (16 to 1) in the collector-to-base current ratios result from the use of the different base contacts (axial or co-axial contact) alone. This effect may possibly find application in control circuits.

Diffusion techniques were applied to an alloyed-emitter--diffused-collector transistor. This construction combines the high injection efficiency of an alloyed emitter with the advantages of the diffusion techniques to obtain a uniformly-flat large-area collector of controlled penetration. Early work reported here has given results comparable to alloyed junction transistors of similar geometry. The diffusion technique has also been applied to obtain a reduction in the base-lead resistance by a factor of 3 through the diffusion of a heavily doped layer in the base wafer before alloying.

Introduction

The extension of the high-current performance of alloyed-junction transistors through the use of high-emitter-efficiency alloys, and the design of high-current and high-voltage power transistors have been discussed previously.[1,2] The purpose of this bulletin is to discuss recent results in further extending the high-current and power performance of p-n-p and n-p-n germanium power transistors. This performance has been obtained principally through an increase in junction area, but also through the application of improved alloying and diffusion techniques. Three types of power transistors are discussed. The first two types are p-n-p and n-p-n large-area alloyed-junction transistors; the third type is a hybrid construction consisting of an alloyed emitter and a collector formed by vapor diffusion.

Supplementary techniques for the reduction of base-lead resistance and improvement in the control of junction flatness are also described.

P-N-P and N-P-N Alloy Junction Power Transistors

Transistor Construction

Fig. 1 shows cross-section diagrams of two junction geometries used for both p-n-p and n-p-n experimental transistors. Significant differences between the solid and ring emitter constructions are discussed below. The mechanical design features have been described elsewhere[2] and are also shown for reference in Fig. 2. The high-emitter-efficiency alloys described earlier[1,2] are also used in the present transistors.

Performance

At high current the collector-to-base current ratio depends primarily on the injection efficiency of the emitter which, in turn, varies inversely as the current density. Hence, good injection efficiency at high currents

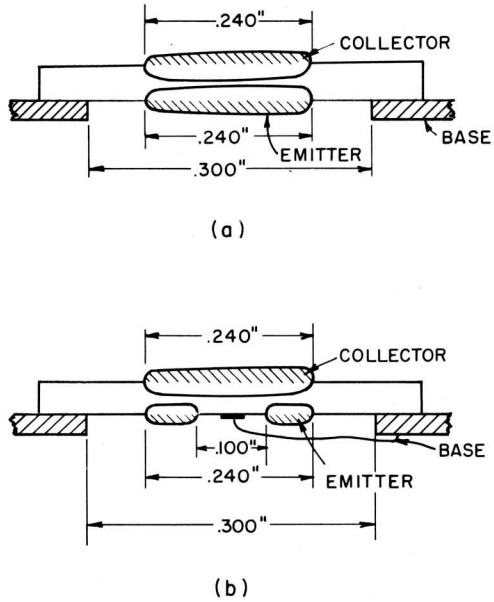

Fig. 1 – Cross-sections of large-area power transistors.

may be obtained by increasing the emitter area to operate with suitable current densities. The achievement of improved operation at higher currents through an increase in junction area can be seen in the curves of Figs. 3a and 3b. Here the collector-to-base current ratio (dc alpha) is plotted as a function of emitter current for p-n-p and n-p-n transistors. The data compare the performance of transistors having a solid 0.060-inch diameter emitter with units having a ring emitter of 0.100-inch and 0.240-inch inner and outer diameters, respectively. The emitter areas are in the ratio of 1 to 15. The smaller-area solid-emitter transistors are those described in reference 2. The collector diameter of the large-area units is 0.240-inch. The curves of Fig. 3a and 3b show that the larger-area transistors are capable of operation with high gain at currents of 10 amperes or more.

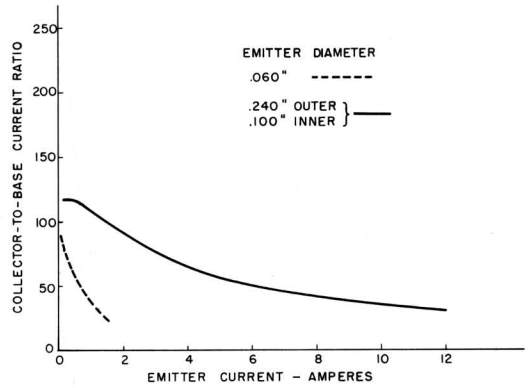

Fig. 3a – Collector-to-base current ratio vs emitter current for p-n-p transistors.

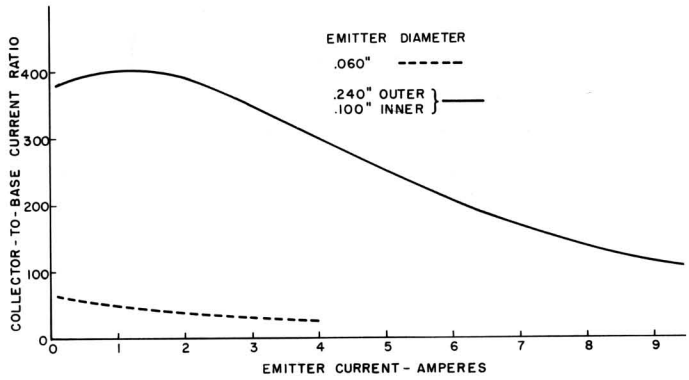

Fig. 3b – Collector-to-base current ratio vs emitter current for n-p-n transistors.

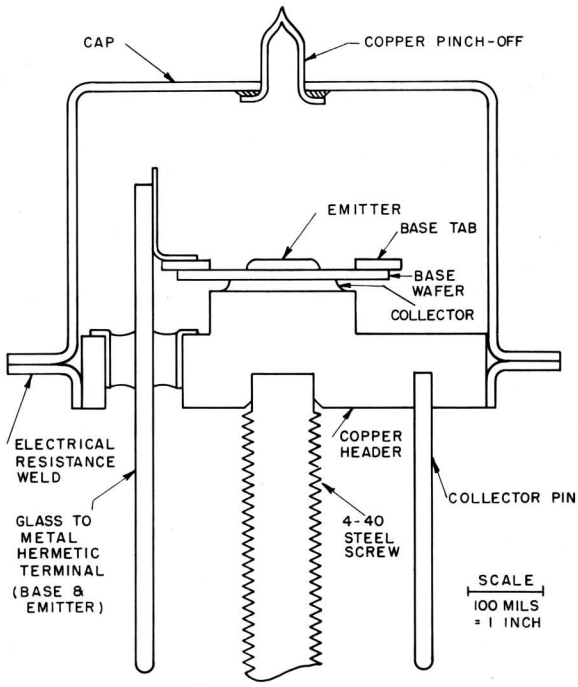

Fig. 2 – Power transistor (cross-section).

Table I shows other electrical characteristics of the p-n-p and n-p-n large-area transistors. Although the large-area junctions present additional wetting and etching problems in fabrication, the data indicate that the techniques used permit the fabrication of these junctions with essentially no degradation in the reverse junction characteristic over that obtained on smaller power transistors[2]. The experimental SX-165 and SX-158 types designated in Table I use germanium of the same resistivity and having similar spacings between junctions. The experimental SX-158A is similar to the SX-158 but modified for higher current and lower voltage operation.

Junction spacings closer than those listed in Table I (about 2.8 mils) have resulted in n-p-n units with 1-ampere current ratios ranging from 200 to 500. A few units have been made with values as high as 1000.

TABLE I

Electrical Characteristics of p-n-p and n-p-n Large-area Transistors*

Experimental Type	Ge base material Resistivity ohm – cm	W (mils)	Collector current with zero emitter current (μa)		Breakdown Voltage	Collector-to-base Current Ratio	
			-1v	-25v		I_c=1 amp.	I_c=10 amp.
SX-158 p-n-p high volt.	4–6	3.3	30	50	125	45	15
SX-158A p-n-p low volt.	2–3	2.5	18	65	60	80	30
SX-165 n-p-n	4–6	3.3	80	120	80	200*	60

*Average values

The increase in junction area also decreases the thermal resistance between the collector junction and the copper mounting stud (Fig. 2). The experimental SX-158 p-n-p transistors have a thermal resistance of approximately 2 to 2.6 degrees C per watt. Most of this thermal resistance occurs in the indium collector dot which is approximately 0.240-inch diameter and 0.010-inch thick. The experimental SX-165 n-p-n transistor, which has a collector geometry equivalent to the SX-158, has a thermal resistance ranging from about 1.8 to 2.1 degrees C per watt. This lower value results from the higher thermal conductivity of the lead-arsenic collector alloy used in the n-p-n transistor. A considerable reduction in the thermal resistance of the p-n-p transistor has been achieved by shaving off approximately three-quarters of the indium collector dot before soldering to the copper stud. Thermal resistance measurements on SX-158A transistors having shaved collector dots range from 0.8 to 1.3 degrees C per watt. These transistors should be capable of operation at power dissipations of 20 to 40 watts, depending upon the ambient temperature.

Alloyed Emitter, Diffused Collector Transistor

The technique of vapor phase diffusion offers important advantages in making large-area power transistors. First, the technique lends itself well to the formation of large-area flat junctions, and to the close control of junction penetration and spacing between junctions. Secondly, it makes possible the elimination of the indium or lead alloy which is the largest source of thermal resistance between the collector junction and the heat sink in the alloyed junction units. Lower thermal resistances should lead to higher allowable dissipation.

In the case of the emitter junction, the results given above demonstrate the high values of injection efficiency obtained with the use of a lead-arsenic alloy. By combining the advantages of an alloyed junction for the emitter with the advantages of the diffused collector, a transistor of improved characteristics may be expected.

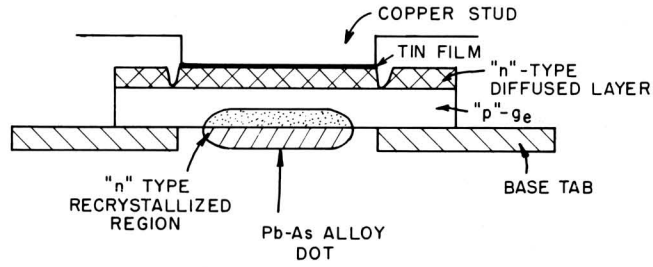

Fig. 4 – Cross-section of alloy-emitter, diffused collector power transistor.

Fig. 4 shows a cross-sectional diagram of an n-p-n transistor of such construction. The emitter is formed by alloying a 0.060-inch diameter 99%Pb-1%As dot at 750 degrees C for 30 minutes. The collector is formed by diffusion in antimony vapor at 820 degrees C for 2 hours. Under these conditions the depth of diffusion is about 1.5 mils. A 0.100-inch diameter tin dot serves as the solder between the diffused surface and the copper mounting stud. Electrolytically etching a groove around the dot through the diffused layer serves to define the periphery of the collector. Table II shows characteristics of these transistors for base materials of two different resistivites. Experience so far indicates that higher breakdown voltages can be achieved with diffused junctions than are obtained with alloyed junctions of the same size using the same germanium resistivity. The high-current transfer characteristics are comparable to those of n-p-n alloyed units of similar geometry described in reference 2. This is to be expected since

TABLE II

Characteristics of alloyed-emitter diffused-collector transistors

Ge. ρ Ω –cm	Sat. Currents (μa)		Reverse Junction Current (μa) (+25 volts)		Breakdown Volts		Collector-to-base Current ratio	
	Emitter	Collector	Emitter	Collector	Emitter	Collector	100 ma.	1 ampere
1.8	14	25	40	35	60	100	70	60
5	50	60	100	100	80	130	80	60

this characteristic is primarily determined by the injection efficiency of the emitter.

A few transistors of this type made with a ring emitter geometry (0.240-inch outer and 0.100-inch inner diameters) and 0.240-inch diameter diffused collectors had current ratios of 100 to 500 at 1 ampere.

The work reported here on this hybrid alloyed-diffused transistor is in an early stage. Measurements of thermal resistance on the 0.100-inch diameter diffused-collector type above have indicated a thermal resistances of approximately 3 to 4 degrees C per watt. This is not better than that obtained with the conventional alloy types[2] having the same geometry. However, refinements in fabrication techniques are expected to result in a substantial improvement in the thermal resistance of this type.

Effect of Location of Base Contact

Interesting observations have been made on the effect of the location of the base contact on transistor operation.

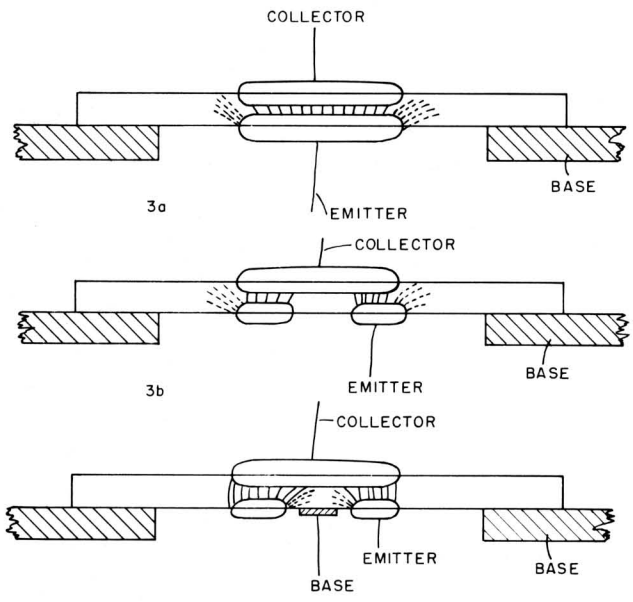

Fig. 5 – Configurations of large-area power transistors.

Fig. 5 a,b, and c show three configurations of large-area power transistors, (a) with a solid emitter (similar to Fig. 1a), (b) with a ring emitter and (c) a ring emitter with an inside base connection in addition to the outside ring base contact (similar to Fig. 1b). In the ring-emitter construction used for transistors described here, the bases are tied together for the purpose of decreasing the base resistance, as shown later. If the two bases in Fig. 5c are not connected, the high-current performance obtained with each base connection differs considerably.

Table III shows collector-to-base current ratios at one ampere for three cases.

TABLE III

Collector-to-base current ratios

Outside base	Inside base	Bases tied together
6	100	80

This phenomenon may be explained as follows. In high-current transistor operation, there is an electric field transverse (parallel to junction plane) in the base region due to the base current and resistance. This field is sufficiently strong and in such a direction as to cause minority carriers injected at the edge of the junction to acquire a drift component towards the base contact. These deflected carriers do not reach the collector and are lost by recombination. For instance, in the case of the n-p-n transistor, the base is positive with respect to the emitter, thus pulling the electron minority carriers toward it. The dotted lines in Fig. 5a represent the flow paths of the current having a drift component toward the base contact while the solid lines represent the diffusion current toward the collector. Now, if the center portion of emitter is removed as in a ring emitter, two factors tend to cause a decrease in gain. First, the current density is increased for a given current. Secondly, much of the minority carrier flow leaving the emitter will occur around the periphery of the junctions increasing the effective spacing between junctions. If, however, as in Fig. 5c, a base contact is placed inside the emitter ring, the transverse electric field in the base is now in such a direction to pull the current carriers inward toward the

center; thus few carriers are lost around the edges. With the two base connections tied together an intermediate condition is obtained as indicated by the data of Table III.

According to this explanation the small-signal current-amplification-factor at low currents should be independent of the base contact position since, at low currents, the electric field in the base region will be very small. Measurements confirm this expectation; α_{cb} at 1 milliampere is approximately the same regardless of the base connection used.

This phenomenon does not occur if the collector is larger than the emitter since the larger collector would catch most of the carriers leaving the emitter. Measurements on transistors having a 0.240-inch diameter collector and emitter of 0.15-inch outer diameter show no difference in current ratios between the inner and outer base connections.

Supplementary Techniques

Reduction of base lead resistance

The base lead resistance ($r_{bb'}$) at high currents can be reduced considerably by reducing the extrinsic portion which exists between the junction edges and the base connection. This resistance remains relatively constant at high currents while the intrinsic base resistance which exists between the junctions decreases to very small values because of conductivity modulation. The geometry shown in Fig. 1b offers a method of reducing the base lead resistance by paralleling two extrinsic lead resistance components, that existing between the outer base ring and outer edge of the emitter and the component between the edge of the inside base dot and the inner diameter of the emitter ring. A comparison of the base-lead resistance for the solid and ring emitter constructions of Fig. 1a and 1b for transistors having the same values of junction spacing and germanium resistivities can be seen in Fig. 6 in which I_{base} vs. V_{base} is plotted. The values of $r_{bb'}$ at emitter currents of 1 ampere, computed from the slope of the curve, are approximately 32 ohms for the solid emitter and 5 ohms for the ring-emitter geometry.

Fig. 7 illustrates a second technique for reducing the base lead resistance. This technique has been applied only to the p-n-p type but, in principle, should also be useful for n-p-n transistors as well. In this method, a high conductivity 'n' type layer is diffused onto the conventional 'n' type pellets used for power transistors. The diffusion process is carried out at 750 degrees C for 2 hours in an antimony vapor and results in a layer of approximately 0.0005-inch thickness. Fig. 7a shows

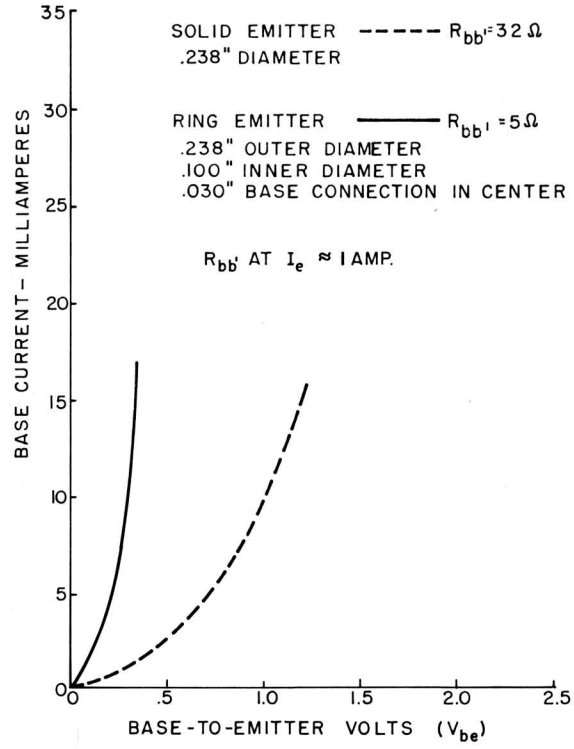

Fig. 6 – Input characteristic of p-n-p power transistors with solid and ring emitters.

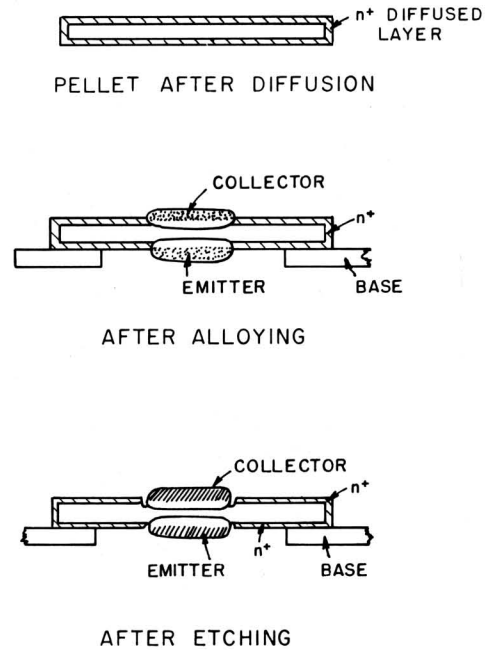

Fig. 7 – Method of reducing base lead resistance.

the pellet cross-section after diffusion. Emitter and collector dots of Ga-In-Au are then alloyed through the 'n' layer at 585 degrees C for 5 minutes as shown in Fig. 7b. The base ring contact is fired on during or subsequent to the alloying process. Finally, the emitter and collector junctions are electrolytically etched to

form a groove around the junctions to isolate the 'n' layer from the 'p' type recrystallized region, thus preserving the breakdown voltages normally obtained with the base germanium used. An alternate technique would be to remove the 'n' layer from the collector side before alloying.

Fig. 7 also shows the final geometry of the transistor. Since the conductivity of the diffused layer near the surface is very high, the base contact has been effectively moved much closer to the emitter region, thus reducing the extrinsic base-lead resistance. The effectiveness of such a process is illustrated by Table IV which gives values of $r_{bb'}$ at 1 ma and 1 ampere for a transistor processed in the above manner. These values are compared with values measured after the diffused layer has been etched away. A substantial increase in the extrinsic value of base resistance has occurred even though the cross-sectional area of the base region was not substantially changed by the light etching used to remove the diffused layer.

This technique was applied to a transistor employing a 0.100-inch diameter emitter, a base ring having an inside diameter of 0.200-inch, and a germanium resistivity of 4 to 6 ohm-cm. The average value of $r_{bb'}$ for units without the diffused layer at 1 ampere was 50 ohms. The average value for units using the pre-diffused pellets was about 20 ohms. This process might be expected to show a comparable improvement in $r_{bb'}$ on transistors having other geometries and resistivities.

Other characteristics such as junction leakage, breakdown, and current transfer ratio are not significantly affected by this process. However, extreme care must be taken in etching to preserve the thin diffused layer on the emitter side.

Methods of Making Large-Area Flat Junctions

Methods of making crystallographically-flat small-diameter alloy junctions have been described[4]. The fabrication of large-area junctions for the transistors described here have been based on conventional alloying techniques. These techniques generally lead to some curvature of the junction front. This curvature effectively limits the value of the spacing between junctions, W, to a minimum. Theoretically, the current amplification of the junction transistor is an inverse function of W.[3] Because of curvature, little is to be gained in high-current performance with larger junction areas if these are obtained at the expense of increased values of the junction spacing. Consequently, new techniques are needed to control the junction spacing by reducing junction curvature.

Efforts have been made in the past to reduce junction curvature by heating and cooling at a slow rate during the alloying cycle to approximate the equilibrium conditions of the alloy-germanium system. Confining the alloy cross-section to a rectangular shape by appropriate jigging, as shown in Fig. 8a also serves to reduce

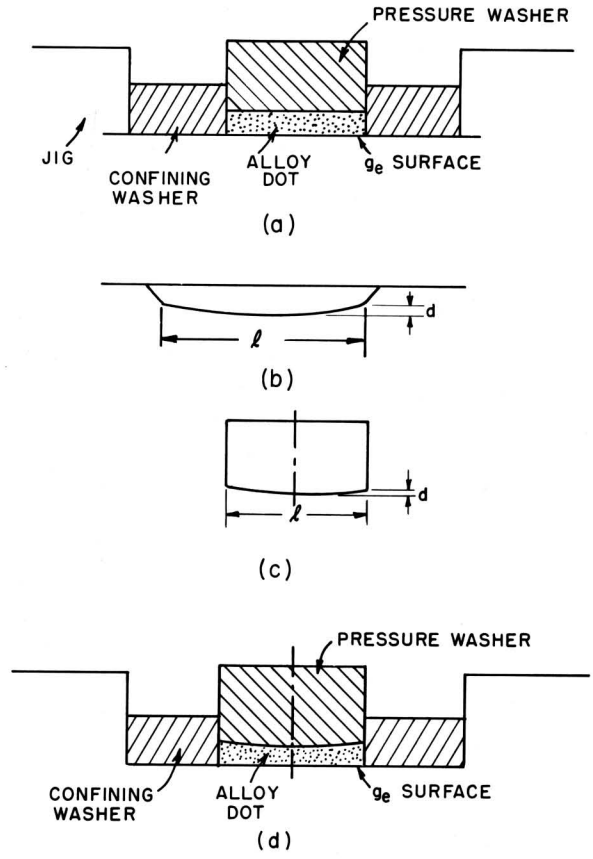

Fig. 8 – Method of obtaining flat large-area junctions.

TABLE IV

Effectiveness of a diffused layer for reducing the base lead resistance

Emitter Current	Base lead resistance With diffused layer	Base lead resistance After removal of diffused layer
1 ma.	80	112
1 ampere	16	50

junction curvature. However, even when these two techniques are used in making large-area alloyed junctions, some curvature continues to exist. This curvature occurs because of the tendency of the molten indium alloy to wet at the center of the dot first, then spread to the edges causing greater penetration at the center.

The depth of penetration of the alloy recrystallization is a function of the thickness of the alloy dot.[5] By changing the shape of the alloy cross section so that the molten alloy is thinner at the center of the dot than at the edges, greater penetration might be expected at the center. This should compensate for the usual tendency toward greater penetration at the center. This compensation may most likely occur when the amount of curvature is a substantial percentage of the total dot thickness, particularly in the case where the ratio of dot diameter to dot thickness is large (25 to 1 for the SX-158 and SX-165).

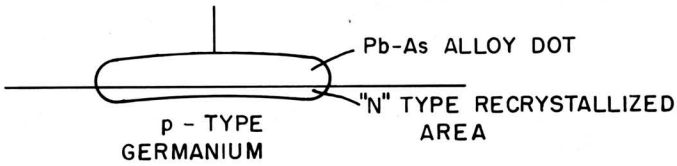

Fig. 9 – Alloy junction made with curved washer.

Large-area junctions (0.240-inch diameter), which were alloyed in a jig similar to that shown in Fig. 8a, were sectioned and the curvature approximated by measuring from a photograph the ratio of d/l (Fig. 8b). This ratio was approximately 0.01 in all cases. As shown in Fig. 8c, the pressure washers were machined to approximate this curvature. The molten alloy then assumes a shape similar to that in Fig. 8d. Fig. 9 shows a diagram of a junction made with the first pressure washer machined in this fashion. It is interesting that the junction is slightly concave, indicating that the curved washer actually overcompensated the normal junction curvature. Fig. 10 shows a photograph of a transistor made with this technique but using pressure washers machined so that overcompensation did not occur. From the photographs it appears that large-area junctions can be made parallel over approximately 75 percent of the diameter by using conventional alloying techniques in combination with compensating pressure washers. These junctions, although relatively parallel, are not flat along the crystallographic plane. This is obvious from the wavy contour of the junction front. More recent work[6] using other techniques in alloying junctions up to 0.100-inch diameter on low dislocation density germanium has resulted in crystallographically-flat junctions.

Using the techniques of Fig. 8, transistors with emitter and collector diameters of 0.240-inch have been made with junction spacings ranging from 0.002-inch to 0.003-inch.

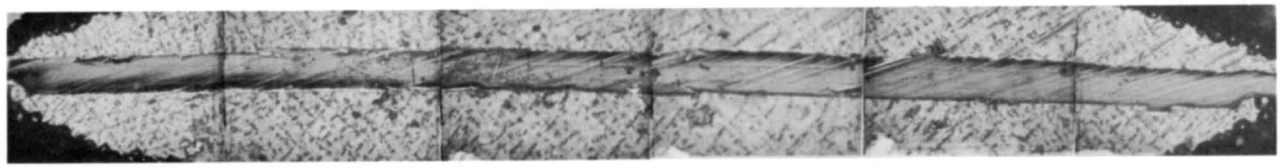

Fig. 10 – Cross-section of large-area p-n-p power transistor (junction diameter 0.240").

J. M. Printon

Bernard N. Slade

References

1. *LB-1013 High-Emitter-Efficiency Alloy Materials for P-N-P-Transistors,* by L. D. Armstrong, C. Carlson, and M. Bentivegna.

2. *LB-1010 Recent Advances in Power Junction Transistors,* by B. N. Slade.

3. *LB-917 On the Variation of Junction Transistor Current-Amplification Factor with Emitter Current,* by W. M. Webster.

4. *LB-990 Uniform Planar Alloy Junction for Germanium Transistors,* by C. W. Mueller and N. H. Ditrick.

5. *RB-23 Calculations of Alloying Depth of Indium in Germanium,* by L. Pensak.

6. RB-72, *Alloying Properties of Germanium Free of Edge Dislocations* by C. W. Mueller.