LB-1040

INTERMEDIATE FREQUENCY TRANSISTOR CONSTRUCTION AND PRODUCTION

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Approved

This bulletin describes the development of an i-f transistor for broadcast receivers that is suitable for mass production. The various considerations involved in the design are presented along with the construction techniques developed for pilot production.

Introduction

The work described in this bulletin had as its initial goal the design of an intermediate frequency transistor suitable for broadcast receivers. This transistor was to have electrical characteristics similar to those of the transistor described in LB-915,[1] but was to be easier to manufacture. All known types of transistors, including triode, tetrode, unipolar, drift and pnip transistors were considered. Since low price was a major consideration, the triode was considered the best possibility. The various methods of making the transistor, such as rate growing, alloying, soldering, surface barrier, diffusion, etc., were considered. The state of the art and prior experience dictated that the exploratory work be concentrated on alloy junctions. The greater technological background available, led to the decision to work only on the p-n-p as opposed to the n-p-n transistor.

Electrical Parameter Target Values

To establish evaluation criteria, the LB-915 transistors used in two types of portable receivers built in the laboratories[2,3] were carefully measured. The electrical parameters were averaged and an allowable spread of ± 20 percent was imposed. This tolerance is similar to that imposed on vacuum tube parameters but at the time it was not known if it would be possible to make transistors to these tolerances. However, this was believed to be a necessary objective if transistors were to be manufactured and used as economically as vacuum tubes. These considerations led to the selection of the target design values shown in Table I.

Table I

Target Electrical Design Values

$r_{bb'}$ = 80 ± 15 ohms

$C_{b'c}$ = 12 ± 2.5 $\mu\mu$f

W = 0.80 ± 0.17 mil

*Figure of merit = 11.6 mc

*Figure of merit = $\frac{1}{4\pi} \frac{g_m}{r_{bb'} C_{b'c} \frac{w^2}{2D_p}}$. The figure of merit and hybrid-π parameters are discussed in reference 4.

As the development progressed minor modifications, reflecting the accummulated experience, were made to these objective values.

The base lead resistance ($r_{bb'}$) and the junction spacing were determined with an input impedance bridge[5]. The 455 kc power gain and noise factor were measured on a unilateralized test set[6]. The value of neutralizing capacity, C_n was used as a measure of $C_{b'c'}$ in this

[1] *LB-915. A P-N-P Triode Alloy Junction Transistor for Radio Frequency Amplification* by C. W. Mueller and J. I. Pankove.

[2] *LB-919. An Experimental Transistor Personal Broadcast Receiver* by L. E. Barton.

[3] *LB-957. A Developmental Pocket-Size Broadcast Receiver Employing Transistors* by D. D. Holmes, T. O. Stanley, and L. A. Freedman.

[4] L. J. Giacoletto, "Study of p-n-p Alloy Junction Transistors from DC Through Medium Frequencies", RCA Review, December, 1954, vol. 15, pp 506-562.

[5] L. J. Giacoletto, "Equipments for Measurement of Junction Transistor Small-Signal Parameters for a Wide Range of Frequencies", LB-900.

[6] T. M. Scott, L. A. Freedman, and D. D. Holmes, "A Test Set for Transistor Performance Measurement at 455 Kilocycles", LB-986.

case they are approximately equal. The gain of a transistor is proportional to the figure of merit in the high frequency region where the gain falls off at a rate of 6 db per octave. The figure of merit is a reliable overall measure of the high frequency performance of the transistor. However, it is not a good measure of transistor reproducibility since the individual parameters of the triple product may change without altering the figure of merit.

General Design Considerations

The simplest triode alloy transistor is the flat wafer type with junctions on either side. The design of the transistor can, in theory, be carried out in a straight forward manner but in actual practice many practical factors influence the decisions that must be made. A brief discussion of the reasons for the design chosen will now be given. Discussion will be limited to practical points not covered in reference 1.

In fabricating close-spaced alloy transistors collector-to-emitter shorts occurred rather frequently. Consequently, a fundamental question that had to be answered was: Can the alloy junction be made flat and the penetration controlled so that the close spacing necessary for the r-f transistor is economically feasible?

A method of making junctions by soldering[7] gave promise. The small junction penetration (0.02 to 0.04 mil) of this technique provided the desired control over junction penetration. However, if a thin flat wafer is used to avoid costly well-forming operations, it becomes difficult to obtain a low base resistance. A combination of soldering and alloying was developed which provided flat junctions with controlled penetration and gave reasonable base-lead resistances using a flat wafer construction.

Junctions made by this combination of soldering and alloying were flat to within 0.02 mil over 90 percent of their diameter (20 mils). Details of making this type of junction have been previously described.[8]

Another factor to be considered is the choice of germanium resistivity, ρ. This influences several parameters as shown below:

Base lead resistance $r_{bb'} \propto \rho$

Collector capacity $C_c \propto \frac{1}{\sqrt{\rho}}$

Breakdown voltage $V_{co} \propto \rho$

As can be seen from the above relationships a decrease in resistivity will decrease $r_{bb'}$ which is desirable but at the same time it will give the undesirable effects of decreasing reverse breakdown voltage and increasing collector capacitance. A resistivity of 1 ± 0.2 ohm centimeter was chosen to give a safety factor in the reverse voltage breakdown. With this choice the collector capacitance is 12 $\mu\mu$f at 6 volts. If low collector capacitance is more important than low base lead resistance, the resistivity can be increased.

Having fixed the resistivity of the germanium, the base lead resistance, $r_{bb'}$ is determined by the geometry. The wafer size must be such that it can be readily handled during processing and measuring. The thickness determines mechanical strength and also the volume of indium necessary to get penetration[9] to secure the correct junction spacing (W). The base lead resistance can be calculated from the formula shown in the appendix. Obtaining accurate results from the formula is difficult because the formula applies strictly at such low currents that there is no conductivity modulation of the region between the emitter and collector. The several thickness measurements must also be known in the finished transistor. This implies knowing the dimensions accurately after the post-alloy electrolytic etch. Since many factors in the processing influence the amount of electrolytic etch required, the actual measurements entering the formula are not known before hand. A safety factor of two to three times must therefore be introduced. Details of this will be discussed later.

Construction

An overall idea of the transistor construction can be obtained from the photograph of Fig. 1 showing the parts and the assembled transistor. Since cost would eventually be the important factor, a simple design was sought for manual assembly. Mechanization was too difficult and involved a task for solution in the time available. Several broad ideas, however, were introduced as described below.

A conveyor type of furnace was considered necessary for production speed and to get a more reproducible control of temperature. Such a furnace was designed and built.

The circular tab (see Fig. 2) for connection to the base germanium was used to obtain a low base lead re-

[7] *LB-1037. The Soldered Transistor* by L. Pensak.

[8] *LB-990. Uniform Planar Alloy Junctions* by C.W. Mueller and N. H. Ditrick.

[9] *RB-23. Calculations of Alloying Depth of Indium in Germanium* by L. Pensak.

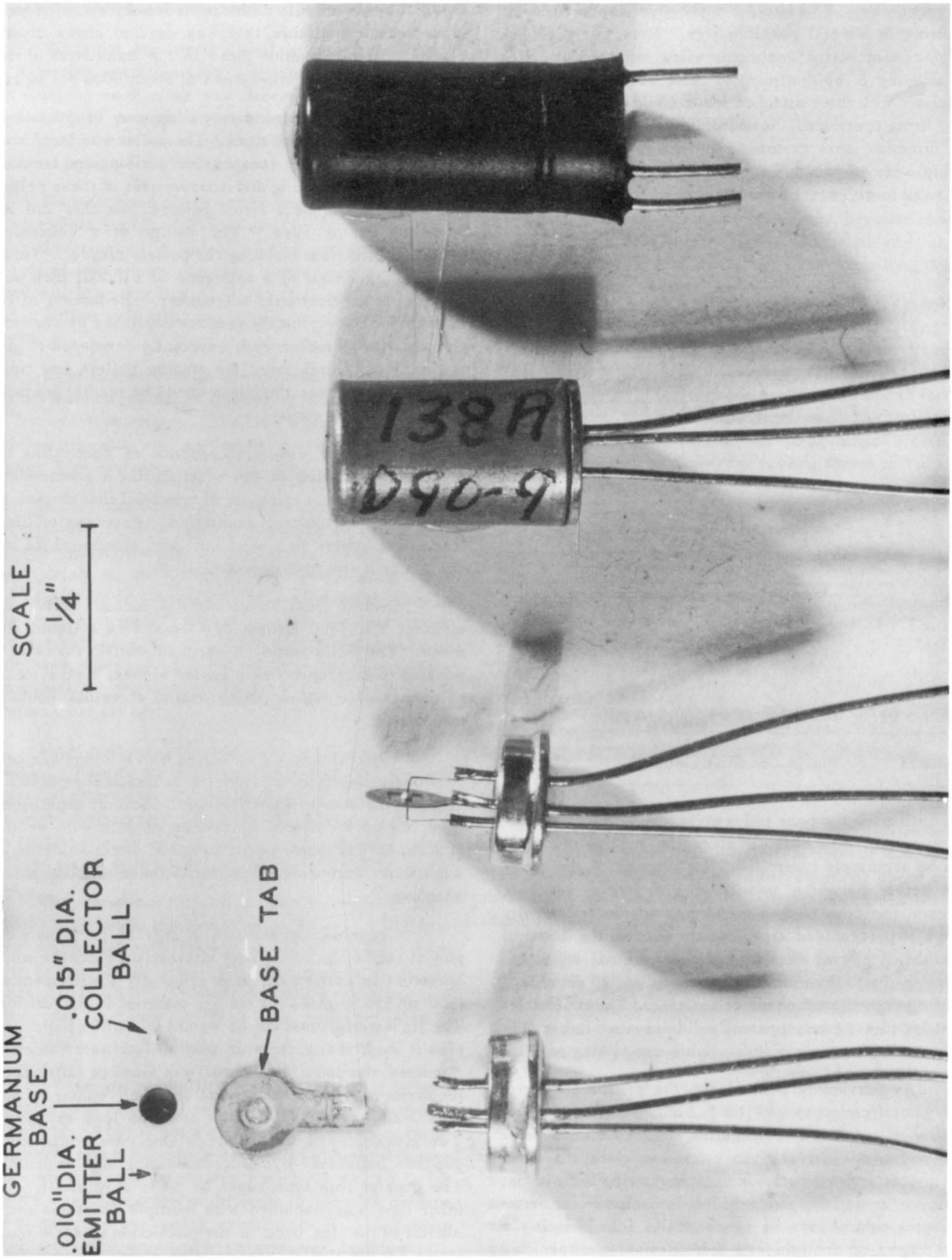


Fig. 1 – Transistor construction.

sistance. The inner depression served to center and hold the germanium. The circular outer edge may be used for centering in several possible jigs. Thus, one might jig the placement of the connector wires into the dots after the alloying or hold wires and base so that a finished transistor with three attached leads could be made in one alloy firing operation. Some preliminary experiments in this direction were performed and these methods of assembly were shown to be possible but the details were not sufficiently worked out for incorporation in a pilot line.

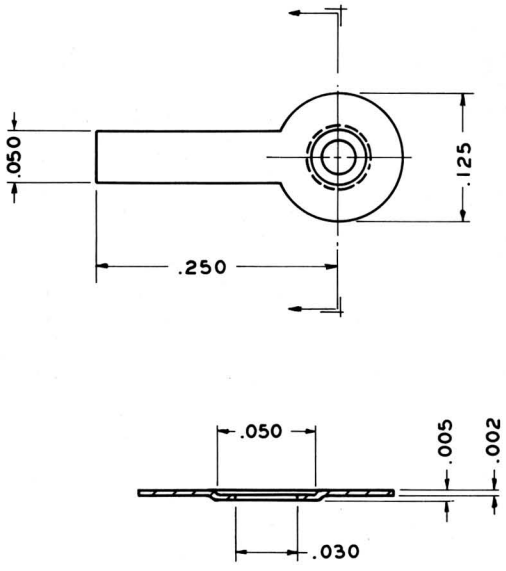


Fig. 2 – Base tab outline.

Coating the base tab with solder, although a simple operation, was difficult since the coating thickness must be accurately controlled. Hot dipping of the metal strip before punching was tried with some success. However, the best method found was to electrolytically plate a 50 percent lead 50 percent tin alloy on the 42-metal base tabs. A plating thickness of about 0.2 mil was used. Soldering the pellets into the base tabs at 500 degrees C in hydrogen gave good ohmic connections. The pellets located by this means apparently did not move in the subsequent alloying operations.

As previously pointed out, the germanium resistivity specification was for 1 ± 0.2 ohm-cm. This specification was difficult to meet for some time because of large variations in resistivity across a crystal diameter. With recent improvements in crystal-growing techniques, a narrower resistivity range which is desirable for better parameter control may be economically feasible. In the early stages of the project a hole lifetime was specified because it was the only criterion of crystal quality available. When a reliable dislocation density counting technique became available, this was used to check crystal quality. The germanium used in the transistors of this bulletin had a dislocation count of about 8000 per sq cm.

The base germanium pellet was 0.050 inch in diameter and 0.002 inch thick. The pellet was later made square in order to use inexpensive scribing and breaking methods. The handling and measurement of these pellets was expected to be a major problem, but this did not prove to be the case. The design of a convenient vacuum chuck made handling the pellets simple. Thickness measurements to a tolerance of ± 0.0001 inch were made with an electronic micrometer. Reduction of the pellet to the correct thickness is accomplished by chemical etching with an iodine etch especially developed to give a slow steady etch rate. By grading pellets and timed etching, the correct thickness could be readily produced in 2 or 3 etching steps.

Since the essential process of controlling the junction penetration is one of saturating a given volume of indium with germanium, it is essential that the volume of the dots be accurately controlled. Punching of discs from sheet indium was used but later abandoned for reasons of cost and poor reproducibility.

Several methods of making indium balls were usable. The final method developed was a liquid shot tower. The balls were selected for correct diameter by passing them through finely graded sieves. By this means an inexpensive and accurate control of volume could be maintained.

The technique of soldering and alloying has been previously described.[8] Here the mechanical problems of aligning the dots will be discussed. Several experiments were run on the direct placement of dots with vacuum chucks, both pressure positioning and direct soldering on a hot wafer were tried. Neither of these methods proved adequate.

Consequently, the use of jigs as previously employed seemed to be the only alternative. Since the solder operation is carried out at a relatively low temperature (300 to 350 degrees C) the jig material is not critical. The jig material must not be wetted by molten indium and also it must resist the flux used to facilitate soldering. Anodized aluminum alloy (dural) was found to fulfill these requirements. Since the dural is much easier to work then stainless steel, the jigs are also less expensive. Two types of jigs were made. One type consisted of punched individual jigs accommodating one transistor. The cost of this type might be made very small. The other type was machined with multiple positions and is similar to the jigs used in the production of audio transistors except that it was made of aluminum instead of

stainless steel. Both types of jigs were usable but the multiple jig was better adapted to rapid assembly.

Since the dots were placed in correct position in the soldering operation only a simple jig that kept units from touching each other was necessary for the alloying operation. In general, a temperature change of 20 degrees C per minute was used for both heating and cooling in the range between 350 degrees to 550 degrees C.

As mentioned above and considered in greater detail elsewhere,[8] a liquid flux is used to facilitate wetting during soldering. The use of a small percent of zinc in the indium dots allows the same wetting action to be obtained with a weaker flux. Alloys of 1/2 to 8 percent of zinc in indium were tried and a value of 1/2 percent was chosen.

Lead connections to the junctions were made in the conventional manner of dipping in flux and soldering in a hot hydrogen stream. The lead wires are 0.003 inch platinum-ruthenium and are indium plated to aid wetting between wire and dot.

In the manufacture of audio transistors a high current electrolytic pulse etch is employed to obtain good collector characteristics. Deep groves, usually a mil or more in depth, are cut around the junctions. These deep grooves aid greatly in overcoming any defects such as dot smearing or edge effects that may have occurred in prior manufacturing. In the high frequency transistor with a thin base wafer and with the requirement of a low base lead resistance, the etching cannot be as vigorous and is therefore more critical.

Many pulse combinations of current and time are possible. Four 50 ma pulses of 2.5 second duration and 7.5 second interval superimposed on a steady 1 ma bias, were found satisfactory. Emitter and collector junctions were pulsed alternatively in this manner. The electrolyte employed was a 40 to 50 percent solution of KOH in water.

The same encapsulation that has proved successful for the audio transistors was adopted. I-F transistors are more sensitive than the audio transistor to proper encapsulation especially with respect to reverse voltage tests. This is probably due to the close spacing between the junctions and base ring and the different processing.

A description of all the experiments tried on both mechanical and electrical problems cannot be included in this bulletin. This is not a serious omission since these experiments may advisably be repeated and yield different results when the test conditions have been altered as for instance when germanium of different dislocation density is employed. In evaluating experiments it is important that all transistor parameters be measured because in a complex device it is relatively easy to move shrinkage from one column to another without improving the overall shrinkage.

Results

Results in a project concerned with the economical production of large numbers of transistors are difficult to evaluate at an intermediate time because the improvement of tools, methods, and techniques goes on all during the development cycle and also for a long period after production begins.

Major emphasis was placed on controlling the transistor parameters important at intermediate frequencies. During one month 600 units were tested. Of this number 320 were rejected because of mechanical failure and poor d-c reverse characteristics. The remaining 280 units were encapsulated and the important electrical parameters determined with the results shown in Table II.

Table II

Percent rejected for each test shown below

No. Electrically Tested	W mil	$r_{bb'}$ ohms	C_n $\mu\mu f$	Unilateralized I-F Gain db
	0.6 to 1.0	50-120	9-14 $\mu\mu f$	39 ± 3 db
280	21%	29%	19%	13%

Since changes in process were continually being made, similar data were plotted in lots of 100 units. Percent rejects varied from 72 to 92 percent of the total number of soldered starts. Distribution curves for the best lot are shown in Figs. 3 and 4.

The distribution curve shown in Fig. 3a is the power gain of the transistors individually adjusted for unilateralization. The gain centers at 39 db which is higher than the original target value of 30 db. This increase in gain is attributed mainly to the unilateralization used.

The distribution of W (Fig. 3b) and C_n (Fig. 4b) shows that a normal distribution is being approached. The base lead resistance, $r_{bb'}$ (Fig. 4a) shows the greatest scattering of all major parameters measured. Some of this scatter is due to variation of germanium resistivity and wafer thickness. However, the major cause of the scatter is thought to be due to variations in the electro-

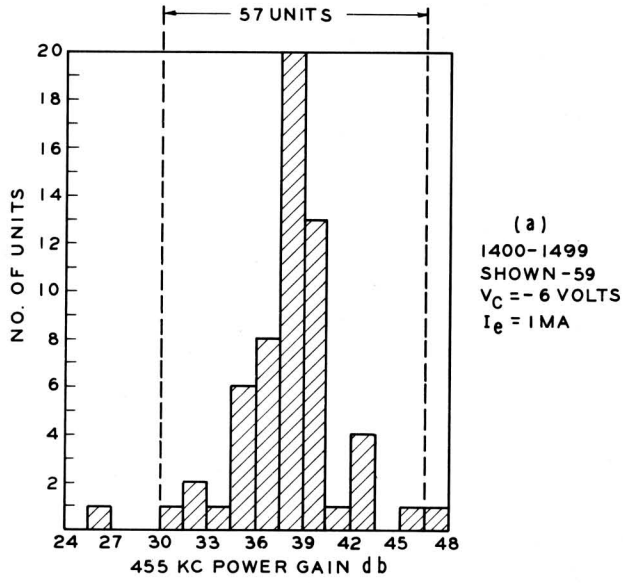


Fig. 3 – a) Distribution of power gain.

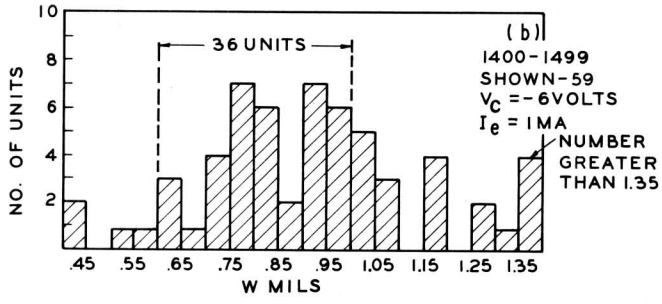


Fig. 3 – b) Distribution of junction spacing.

lytic etch depth. This has an important effect on base lead resistance as is readily seen by examining the formula of Appendix II.

The d-c electrical and mechanical shrinkage of the 600 units mentioned above is shown in Table III.

Table III

Electrical and Mechanical Shrinkage

Starts	Emitter to Base Shorts	Mechanical and Misc. Shrinkage	High I_{co} and/or Low V_{co}
600	18%	14%	42%

The best of the good units had junction saturation currents approximately equal to the theoretically expected value but many rejected units had very high reverse currents indicating the presence of leakage. The high shrinkage on these units can be attributed to several things:

1. The flux was not completely washed off of many units even with the use of ultrasonic agitation.
2. The intense and deep electrolytic etching as used in the audio transistors was not possible because of the thin wafer and close tolerances of $r_{bb'}$ required.
3. The units were particularly sensitive to moisture and hence to encapsulation techniques.

Difficulty with the reverse collector characteristics was now recognized as a serious problem and considerable effort was devoted to it. A technique was developed that gave excellent results and reduced shrinkage due to poor reverse characteristics by a factor of two, an important reduction. This technique consisted essentially of following the electrolytic etch by a benzene rinse and immediate immersion in silicone resin, SR98. This treatment replaced a 24 hour cure in room air. Unfortunately, although many units were satisfactory on life, there were enough failures to cast doubt on the process. Since life tests were somewhat ambiguous, it was felt that this treatment could not be used at the present time. More tests at some future date are desirable.

Life test results carried out at maximum (35 mw) and twice maximum (70 mw) rated power dissipation are summarized in Table IV. These data show that life was generally satisfactory. This result indicates that the flux was completely removed in units which were properly processed. If flux had been partly removed a poor life would have been expected.

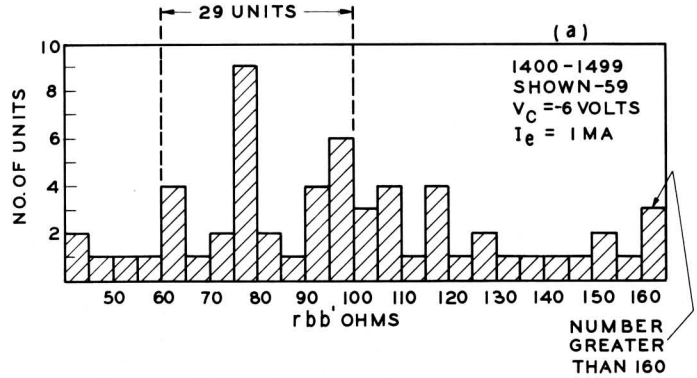


Fig. 4 – a) Distribution of base lead resistance.

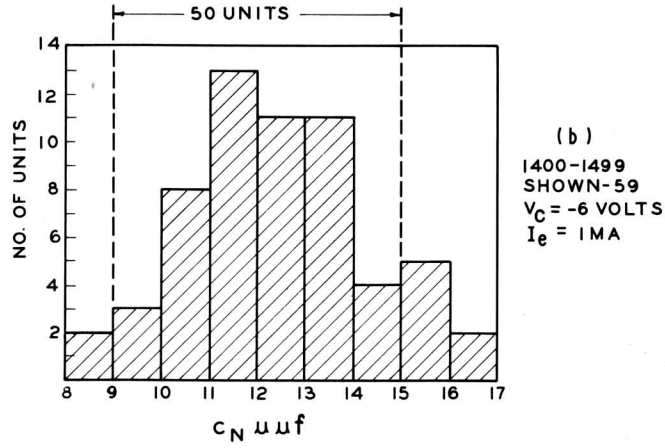


Fig. 4 – b) Distribution of neutralizing capacity.

Table IV

Life Test Summary

Test Conditions	No. Units	No. Hours	No. Failed
P_c = 35 mw, V_c = -12 v, T = 25°C	10	1005	0
P_c = 35 mw, V_c = -12 v, T = 25°C	10	505	0
P_c = 70 mw, V_c = -12 v, T = 25°C	10	156	1 (V_{co} dropped 24 v to 10 v)
Shelf life T = 85°C	10	976	0

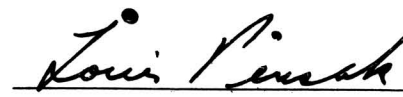
On the last group α_{cb} dropped from an average of 54 to 41. However, because of the design, the unilateralized i-f gain remains unchanged.

Summary and Conclusions

A flat wafer transistor design with a ring base tab was developed which met all the desired electrical characteristics and was relatively simple to manufacture.

A method of making planar alloy junctions flat to within 0.02 mils was developed and incorporated into the transistor manufacture.

A complete pilot line with jigs, furnaces, controls, and measuring equipment was set up on a small scale. It was demonstrated that a transistor could be made in which pertinent r-f characteristics would be controlled to the same degree (±20 percent) as is done in the manufacture of vacuum tubes. Rejects for each important parameter varied between 15 and 25 percent. Because of the many parameters tested overall percent rejects on 100 units was 72 percent.



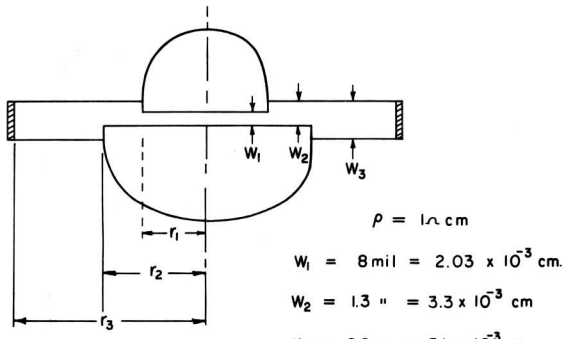
Louis Pensak

C. W. Mueller

Appendix I

Base Lead Resistance

The base lead resistance can be readily calculated from the idealized geometry of the transistor (Fig. 5). In this formula[10] – the reduction of resistance caused by conductivity modulation of injected carriers at the emitter is neglected. The transistor is divided into three regions that are evident from the drawing. The first term is similar to point contact spreading resistance and is the term most subject to conductivity modulation. The second and third terms are the resistances of the germanium between concentric rings. It is instructive to note the relative values of these terms for the i-f transistor as shown. Each term is inversely proportional to the thickness associated with it. The values of W_1 and W_2 are changed by the alloying conditions; W_2 and W_3 by the electrolytic etching.



$\rho = 1\,\Omega\,cm$

$W_1 = 8\,mil = 2.03 \times 10^{-3}\,cm.$

$W_2 = 1.3\," = 3.3 \times 10^{-3}\,cm$

$W_3 = 2.0\," = 5.1 \times 10^{-3}\,"$

$r_1 = 7.\," = 17.8 \times 10^{-3}\,"$

$r_2 = 11.\," = 28. \times 10^{-3}\,"$

$r_3 = 15.\," = 38. \times 10^{-3}\,"$

$$r_{bb'} = \rho \left[\frac{1}{8\pi W_1} + \frac{1}{2\pi W_2} \ln \frac{r_2}{r_1} + \frac{1}{2\pi W_3} \ln \frac{r_3}{r_2} \right]$$

$$= \rho \left[20 + 21.8 + 9.7 \right]$$

$$= 51.5 \text{ ohms}$$

Fig. 5 – Base lead resistance calculation.

[10] J. M. Early, "Design Theory of Junction Transistors", *BSTJ*, Vol. 32, p. 1271, November, 1953.

Table V shows the large effect that the weak electrolytic etch, as described herein, has on the characteristics of 6 transistors. The value of $r_{bb'}$ is increased by 50 to 90 percent. The change in capacitance is probably due to a reduction in area. These particular units were made by direct hydrogen alloying rather than the solder down process and probably have a tapered junction at the periphery. This could account for the change in effective "W_1" that was measured.

Table V

	B	B	A	B	A	B	A
	$\mu a.$	ohms	ohms	$\mu\mu f.$	$\mu\mu f.$	mils	mils
Transistor	I_{co}	$r_{bb'}$	$r_{bb'}$	C_c	C_c	W_1	W_1
1097	1.0	27.5	43.5	15.9	14.0	1.13	0.91
1098	2.0	58.	110.	12.9	10.0	0.53	0.46
1099	1.4	136.	185.	13.8	12.3	–	–
1100	1.4	34.	51.	17.4	16.0	1.05	0.96
1101	1.0	34.5	51.5	20.0	15.0	1.26	1.16
1102	2.4	43.5	66.5	14.8	12.2	0.63	0.48

B = before electrolytic etch

A = after pulse etch as described in main text

Collector Capacitance

The important capacitance in the i-f transistor that must be carefully controlled is $C_{b'c}$, the feedback capacitance in the π equivalent circuit. $C_{b'c}$ is very nearly equal to C_c, the depletion layer capacitance of the collector junction. The C_c capacitor is similar to that of a conventional capacitor with an area equal to that of the junction, and a spacing determined by the depletion layer which in turn depends on reverse voltage. It should be noted that the total area is involved.

For a *flat* circular junction:

$$C_c = 0.07 \frac{d^2}{[\rho V]^{1/2}}$$

where C_c = capacitance in $\mu\mu f$

d = diameter of junction in mils

ρ = resistivity of base in ohm cm

V = reverse voltage in volts

A convenient set of curves of this function is plotted in Fig. 6. The actual transistor junction, however, is not entirely flat and for an exact calculation the sides of the recrystallized volume as shown in Fig. 6 should be included.

A good rule of thumb for the i-f transistor described is that the effective diameter is approximately 1 mil larger than the diameter (d_s) measured at the surface, i.e., a measured d of 21 mils means a capacitance corresponding to 22 mils on the chart.

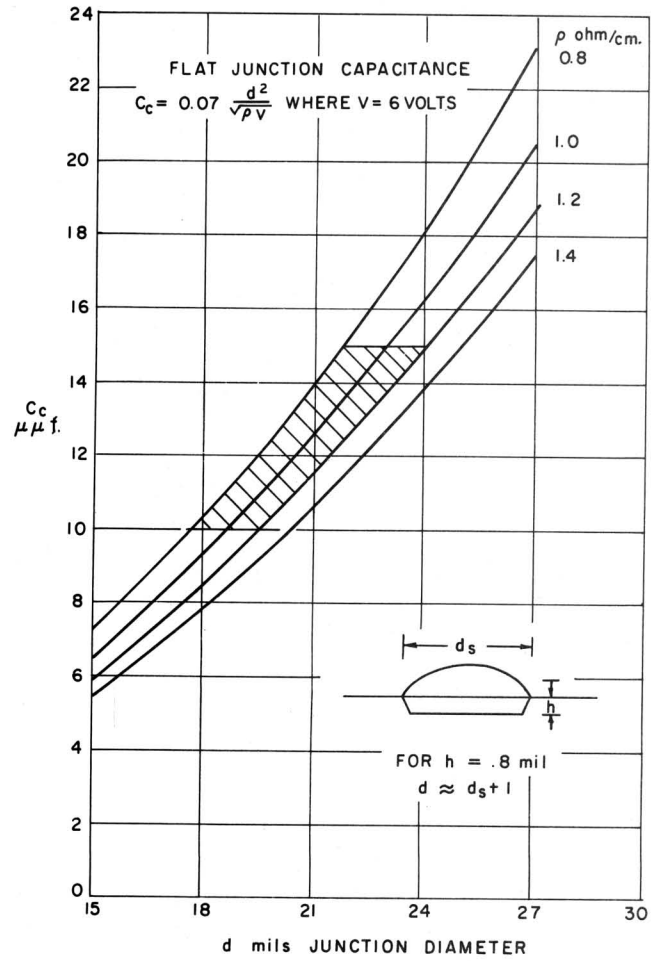


Fig. 6 – Variation of collector junction capacity with collector diameter.