LB-1037

THE SOLDERED TRANSISTOR

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Approved

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This bulletin describes the fabrication of transistors with soldered junctions using a low temperature and a flux in air, rather than a high temperature in hydrogen as in conventional alloy techniques.

Introduction

This bulletin will describe a transistor fabrication technique which resembles the familiar techniques used in soldering of metals. Hence the name soldered transistor. The process is characterized by the use of a chemical flux to promote wetting and to shield against the oxidation effects of air. The activity of chemical fluxes can become effective at lower temperatures than are required with hydrogen and the low temperature makes possible wetting of dot material to germanium with practically no penetration.

The use of the solder process for transistor junctions dates back to the work of C. W. Mueller of this laboratory who successfully made junctions with it several years ago. This effort was revived as a by-product of the use of the solder process in making ring shaped junctions for a unipolar transistor.

The Solder Process

The solder process is the name for a number of improperly understood mechanisms by which a chemical can act on the surfaces of a solid and a liquid metal to promote a cohesive action which is called "wetting". The theory of the interaction of clean metals in reducing or inert atmospheres is reasonably well understood.[1] However, the action of chemical fluxes seems to require extensive experimentation in order to get anything like a complete picture of the process. Effects that prevent wetting are better understood than those that promote it[2]. In spite of the incomplete understanding of the solder process, transistors can be and have been made using such a process.

1. A. Bondi, "The Spreading of Liquid Metals on Solid Surfaces", *Chem. Reviews*, V52, p. 417, April, 1953.
2. G.L. Bailey and H.C. Watkins, "The Flow of Liquid Metals on Solid Metal Surfaces and its Relation to Soldering, Brazing, and Hot Dip Coating".

The procedures involved are as follows. A wafer of germanium is etched as in preparation for making an alloy junction. A base tab is attached by soldering. For n-type germanium, this tab is of nickel or other suitable metal and is coated with a solder of 49 percent lead, 49 percent tin, and 2 percent antimony. The tab may be dipped into flux before placement in contact with the wafer or flux can be added after contact. The amount of flux is not critical. Satisfactory results have been obtained with Divco No. 229 flux, although Divco No. 335 flux is also suitable. On heating in air to a temperature of 250 to 300 degrees C, the solder effectively bonds to the germanium and forms the desired contact. For experimental purposes, a heating device called a "hot tweezers" has been used. This is simply a small clamp made of nichrome ribbon so mounted that it can be heated by passing current through it. This is used to clamp the base tab and wafer together during heating and thereby serves both as a support and heat source for soldering. The device is also small enough to fit under a microscope for examination of the soldering operation. A thermocouple is welded to the nichrome ribbon to give an approximate indication of the temperature.

The transistor junctions are made by soldering indium dots on opposite sides of the germanium wafers. Indium dots of the size desired are prepared. Their initial shape is not important because they will assume a spherical shape when heated to the melting point. The dots are covered with flux. Best results for soldering indium were achieved with the use of Divco No. 335, a zinc-chloride type flux. One drawback to this flux is that it loses its water at 100 degrees C and becomes a dry crystalline mass which does not melt until about 180 degrees C. In drying it may raise the indium off the germanium and move it around somewhat. When the flux melts, the dot, now a molten sphere, touches the germanium and begins to wet. At a temperature of 250 degrees C the dot appears to be fully spread out.

The emitter and collector dots can be soldered in sequence by simply turning the wafer over and reheating. The dots are, of course, placed opposite one another. The second dot can be positioned by jigs, optical refer-

ences, or in a depression formed by electrolytic etching. This latter method consists of mounting the wafer on a stem, soldering on one junction and connecting it to a stem lead. The assembly is then dipped into an alkali bath and the diode operated in the forward direction for a short time. The germanium surface opposite the junction is selectively etched to produce a shallow etch pit of the diameter of the junction. The second junction can be located with respect to the etch pit and soldered in place without affecting the earlier junction.

Soldered Transistor Results

Transistors made with indium on 3 ohm-cm n-type germanium showed rectification and saturation currents comparable to that found with alloyed junctions. Comparable emitter injection efficiencies were also found. Units made on germanium wafers 3 mils thick gave performance that was normal for a transistor of this rather large base width. With a base width of 0.5 mils and 10 and 15 mil dots, good high frequency performance was obtained. The gain at 1 mc was 25 db and almost 10 db at 10 mc. This, too, is comparable with the performance of alloyed junction transistors of similar dimensions. Thus, the electrical performance of soldered transistors is similar and equivalent to that of alloyed junction transistors of similar dimensions. However, differences do exist in the fabrication technique; some of these differences are advantageous and some disadvantageous.

One advantage is that of reducing the problem of control of alloying depth. This occurs because the total penetration of the soldered junction is in itself very small. To obtain a controlled small base thickness in the alloyed junction transistor, in which the penetration is much greater than in the soldered transistor, requires control of dot size, dot spreading, and temperature[3] in addition to initial wafer thickness. For example, in the r-f transistor of *LB-915*[4], if the solder process were to be used and the thin part of the wafer thickness were to be controlled in the range of a half mil instead of the two mils, the other factors would become less critical. Dot size and spreading would then affect only junction capacitance rather than both the capacitance and junction spacing. The firing temperature in the solder process can vary 50 degrees without seriously affecting the junction spacing.

A characteristic which must be considered is a possible increase in base lead resistance due to the smaller wafer thickness. Too few transistors were made to evaluate the magnitude of this effect. The method, which was employed on the *LB-915* transistor was to keep the wafer thick and to drill or etch wells in the wafer. The dots could then be soldered in the bottom of the wells. Another method is to bring the base contract up close to the junctions by the use of a novel electroplating technique described below.

Special Techniques

Electroplating of Base Connection

This new method of forming the base connection is a means of plating metal over the crystal surface up to but not touching the junction. The assembled transistor is immersed in a plating bath, such as the sodium stannate bath for tin, or a copper cyanide bath for copper. The base is made the cathode of the bath and plating occurs on the germanium. The junctions, however, are connected to the anode. Potential differences now exist in the base wafer ranging from cathode to anode. It is well known that, for most plating baths, a minimum potential difference exists below which plating cannot occur. Thus, the areas close to the junctions within this minimum potential difference from the anode will not plate while the remaining area up to the base connection will plate. The plated metal will therefore cover all the germanium around the junction but stop short of it approximately in the shape of the junction contour. The distance between the edge of the plating and the junction can be made small by setting the junction potential close to the minimum plating potential.

The use of an antimony-tin plating bath for p-n-p transistors gives a rectifying instead of ohmic contact directly after plating. This is corrected by a quick heating to the melting point of tin which fuses the plating to the crystal and removes the surface barrier. There is some evidence that copper plating on a p-type crystal may provide ohmic contacts without the need for heating and so be suitable for n-p-n transistors. However, this has not been tried. Another problem exists in the choice of a plating bath. Directly after plating copper on a p-n-p transistor a simple water wash was sufficient to restore the good rectification characteristics of the junctions. It is probable that there was some etching around the junction during plating. However, after plating with tin, the junction acts shorted. To correct this by sufficient etching in acid or alkali to restore the junction is also sufficient to remove the tin plating because the tin is so chemically reactive. One test of the addition of sodium cyanide to the tin plating bath showed no need for subsequent etching and therefore provides a hope that a plating bath for tin can be found that will etch as well as plate simultaneously.

3. *RB-23 Calculations of Alloying Depth of Indium in Germanium.*
4. *LB-915 A P-N-P Triode Alloy Junction Transistor for Radio-Frequency Amplification.*

Etching Pellets To Size

The problem of preparing thin germanium for the soldered transistor can be met by several procedures. Thin wafers are very fragile and present techniques tend to prefer thin regions in thicker wafers. This implies well drilling, either by ultrasonics followed by acid etching, or direct etching with streams of electrolyte. The latter method seems most promising provided a method is used for measuring thickness during etching, and at least three such possibilities are known. One can use an infrared light transmission method, or a depletion layer method (which was used to make the high frequency transistor described above), or an x-ray transmission method.

The infrared light method was described by Evers, et al., at the IRE Conference on Semiconductor Device Research in June of 1954. The wavelength used was 1.38 microns which was called an optimum value. The light was sent through the crystal and its intensity compared with a fixed beam. The crystal is etched until a given light transmission is observed. This method appears to be applicable to thicknesses under 0.5 mils. The variation of the surface reflection coefficient may introduce deviations from the relation between transmission and crystal thickness but this may not be serious.

The x-ray method is free from errors of this type. By choice of the x-ray target for preferred wavelengths, the range of measurements can be extended to include several mils as the upper limit. A preliminary study has shown that the x-ray beam intensity can be stabilized to a high degree, that scintillation counters will be fast enough and that electrolytic etching can be done during measurement. The set-up is moderately expensive (over $10,000 for the x-ray system alone) and will take some development work to make it a reliable tool. It has not yet been set up in any form which includes the etch process.

The depletion layer method is attractive as a research tool but may even be of value in production. Its use is restricted to the p-n-p transistor and to a maximum thickness less than the maximum thickness of the depletion layer of a reverse-biased junction. It requires that the base connection and one of the junctions are in place, etched, and protected so as to be electrically operative. A stream of electrolyte is projected on the face opposite the junction. An etching current is passed between the electrolyte and the wafer. With a d-c bias applied to the junction, the etching will proceed until the depletion layer equipotential surface corresponding to the etch potential is reached. Since the etch pit starts with a rounded bottom, the etching stops first in the area of maximum penetration and then tends to flatten out to the shape of the equipotential surface. If the etching is allowed to procede without limit it will eventually remove the junction from the base by following the equipotential contour to the opposite surface of the wafer. To prevent this, one can stop the etching at a given time, determined by experience, after the depletion layer is first exposed. Because the initial crystal thickness may not be accurately known, the time of etching to penetrate in to the depletion layer is not readily predicatable and it may be the major part of the time of etching. It is desirable, therefore, to ignore the measurement of this time and to obtain a signal that indicates the initial exposure of the depletion layer.

An initial exposure indication can be generated as follows. A curve tracer circuit is arranged to present on an oscilloscope the voltage-current characteristic of the junction at a 60 cycle rate. The desired final thickness can be set, as was seen above, by the d-c junction voltage required to give a depletion layer of that thickness. The maximum curve tracer voltage is set to be well above the necessary d-c voltage. Thus the depletion layer thickness varies from zero to more than the desired value at the curve tracer rate of 60 times a second. The saturation current of the junction should be essentially constant. The projection of a beam of light onto the etched surface increases the junction saturation current because of the generation of electron-hole pairs in the surface. When the etching voltage is turned on, it produces a field at the surface in the direction of removing some of the light-generated holes and thereby reduces the saturation current. As etching proceeds, the saturation current curve is unchanged just so long as the depletion layer does not reach the etched surface. However, when the etching has gone deep enough, the field of the depletion layer at maximum voltage not only reaches the etched surfaces but also dominates the field due to the etching voltage and collects some of the light generated holes. This results in a small jump of current near the maximum voltage swing. As etching reduces the wafer thickness, the current jump is seen to move to lower values of junction voltage. The desired d-c voltage can be switched on when the jump occurs at the corresponding voltage on the curve tracer, and time is measured from this point. The thickness of the depletion layer will correspond to the value of the d-c voltage minus the etch voltage. If a junction is to be soldered onto the etched surface, some allowance must be made for the small penetration of the solder dot. The depletion layer will reach the new soldered junction with about 2 volts less than the final d-c bias used to stop the etching.

Summary

The existence of a choice of methods for obtaining the necessary thin sections in germanium wafers makes

possible the use of soldered junctions for transistors with their possible advantages. Such junctions have been shown to be electrically equivalent to alloy junctions for frequencies from audio to the megacycle range. Where they were put on diffusion doped wafers as for the drift transistor (*LB-1018*)[5] gains of 18 db at 40 mc were obtained. The solder process can therefore be said to be an alternative method of making transistors.

5. *LB-1018, The Drift Transistor.*

Louis Pensak